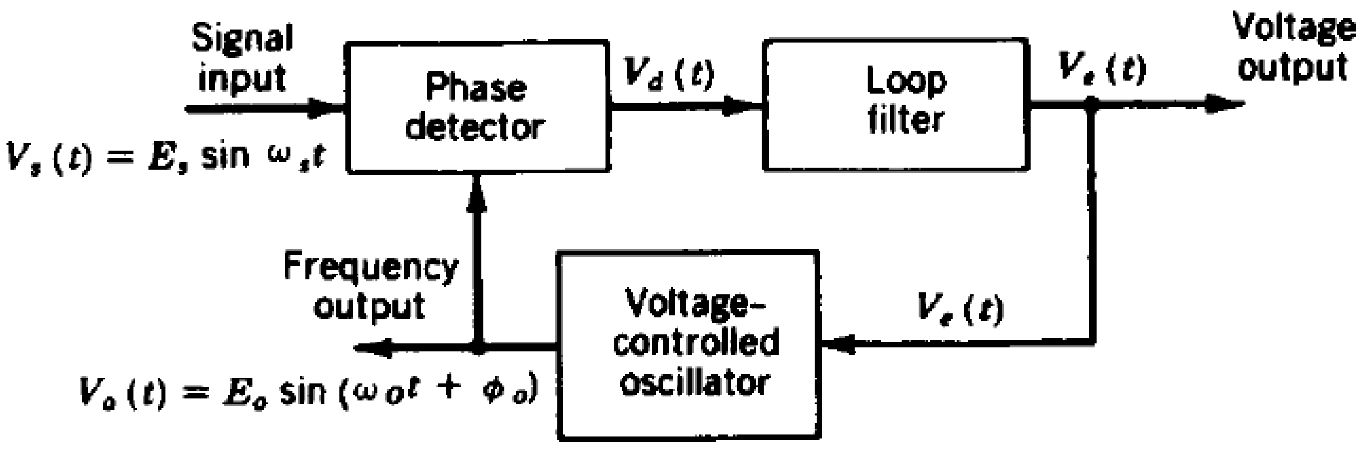
Phase Locked Loop

- The PLL is a frequency-selective feedback system that can synchronize with a selected input signal and track the frequency changes associated with it.
- Its applications span in the transmitter as frequency reference, in receiver for carrier reconstruction and in general for synchronization purpose.
- It provides high noise immunity and very narrow bandwidth
- The basic PLL is comprised of 3 blocks:
  - A phase detector
  - A loop filter
  - A voltage controlled oscillator (VCO)

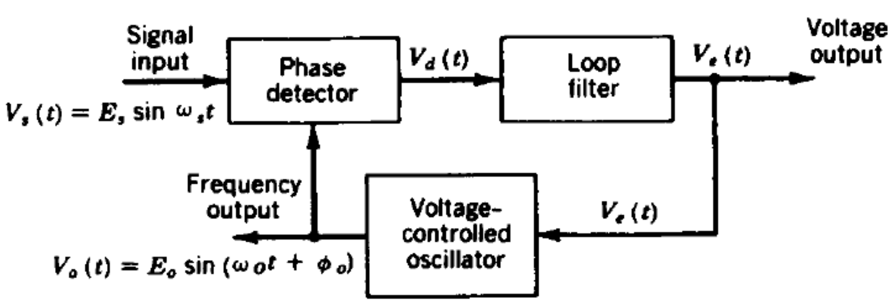
Phase Locked Loop

- The phase detector compare the phase of a periodic input signal, Vs, with the output signal of the VCO and generate an error voltage, Vd.
- This voltage signal is then filtered by the loop filter and applied to the VCO in the for of an error voltage, Ve, to control its frequency of oscillation



Phase Locked Loop

- Voltage output
  - When the PLL is locked, Ve is proportional to the frequency difference between Fs and the free-running VCO freq. F0. Thus the voltage output serves as frequency discriminator and converts the frequency changes in voltage changes.
- Frequency output
  - When the PLL is locked on and input signal, the VCO provides an harmonic signal at exactly the same freq. as the input freq, except for a phase ϕ0, which is necessary to generate the error voltage. This is used to regenerate a weak signal

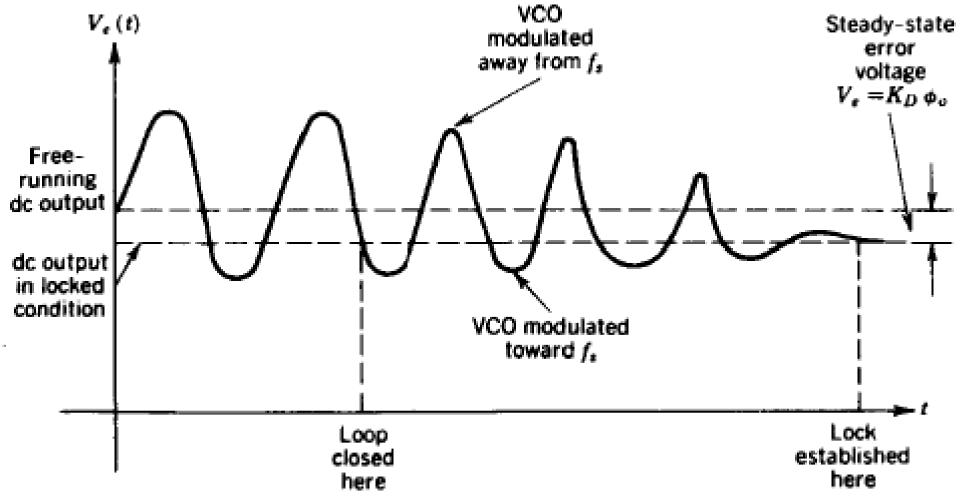


Phase Locked Loop - Capture

- The phase detector (PD) normally functions as a mixer producing

$$\Delta f = |f_o - f_s|$$

- If the difference is sufficiently small it passes through the filter, this is the waveform:



- The waveform contains a dc voltage components that steadily pushes the VCO freq. toward the input signal.

Phase Locked Loop - Capture

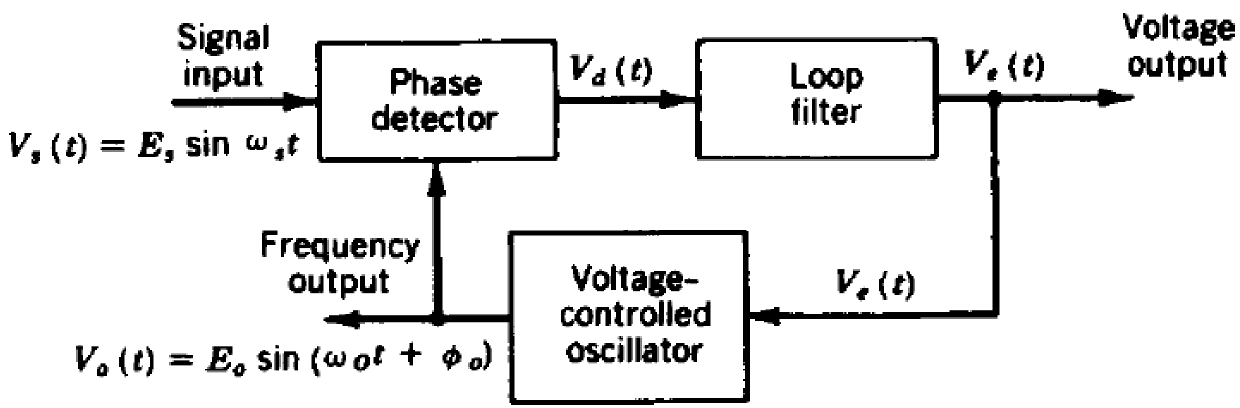
- Once the system is locked the difference frequency is zero and only the dc component remains.
- This dc is generated by the phase difference between the phase difference, ϕ_0 between the VCO and the input signal

$$V_e = V_e(t)\Big|_{\text{steady state}} = -K_D\phi_o$$

- Because the loop filter, the PLL captures only those signals that are close to the VCO free-running freq such that the difference frequency Δf falls approximately in the bandwidth of the loop filter.

PLL - loop filter

- The reduction of the loop filter bandwidth has the following effects on the system performance:
  - The capture process become slower
  - Capture acquisition range decreases
  - Interference-rejection improves
  - The transient response to sudden change of the frequency changes of the input frequency within the capture range become underdumped



PLL – tracking characteristics

- Once PLL is locked is can track small freq changes of the input signal generating additional phase error ϕ_0.
- The loop function as a frequency-voltage converter
- The tracking range is determined by the maximum Ve can be generated internally, normally this value is reached when ϕ_0 has reached the limiting value of ± π/2 rad

$$\pm\,\Delta f_L = \pm\,(V_e)_{max} K_0$$

- Where K0 (Hz/V) is the VCO gain

PLL – tracking characteristics

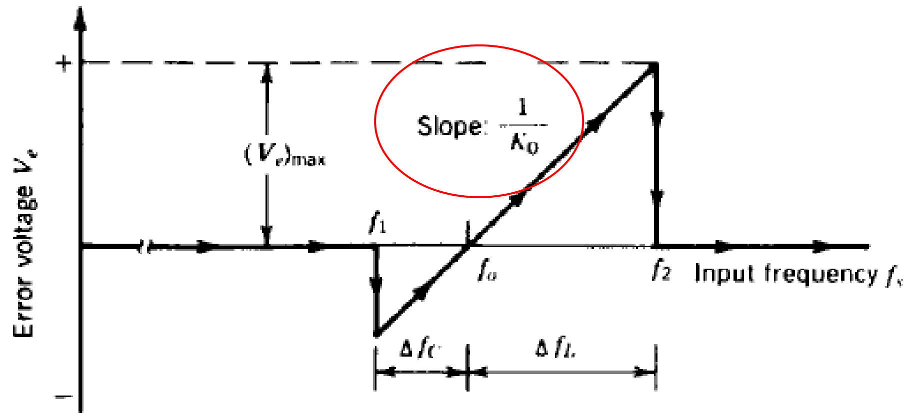
- Typical PLL freq-to-voltage transfer characteristics: slowly increasing and decreasing input frequency.

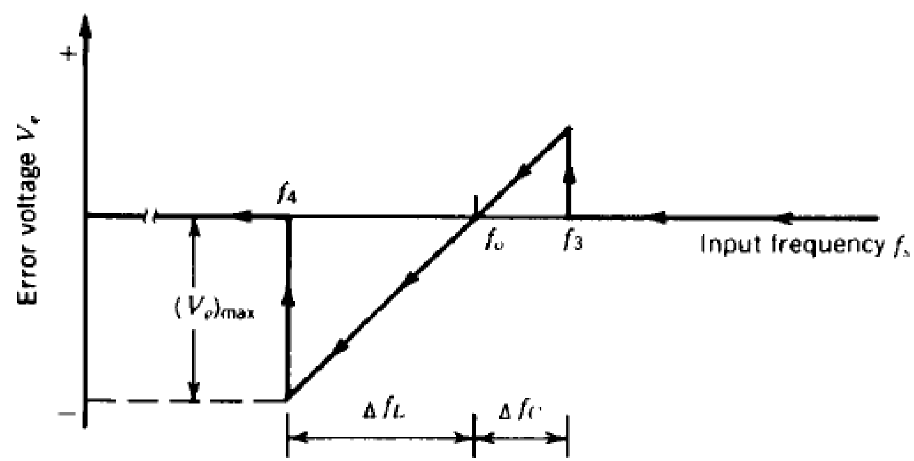
- Capture range:

$$f_3 - f_1 = 2\Delta f_C$$

- Tracking range:

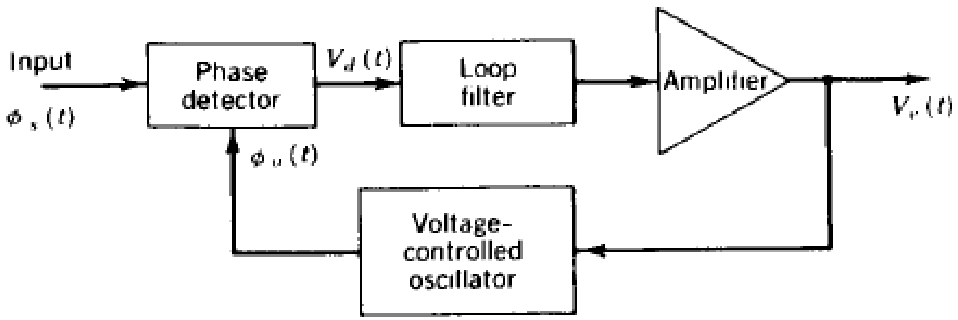
$$f_2 - f_4 = 2\Delta f_L$$

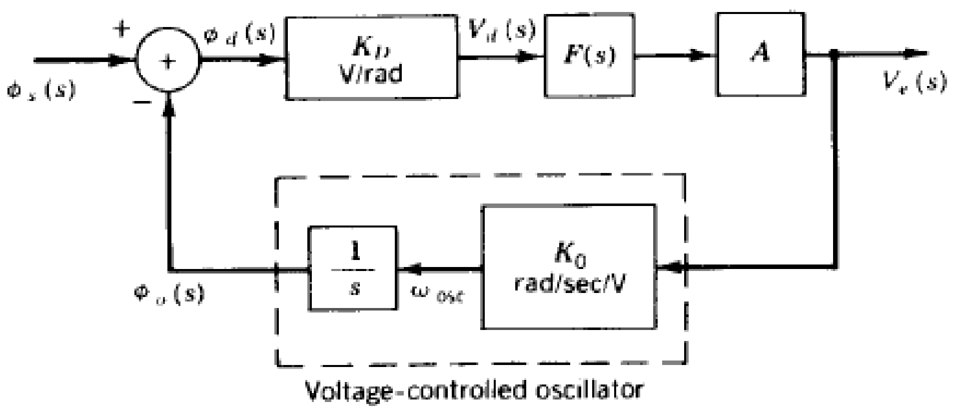




PLL – in locked condition

- In locked condition a linear relation exists between the output of the phase detector and the phase difference between the two.
- The PLL is analyzed as a feedback system in the complex frequency domain $s=\sigma+j\omega$.





PLL – in locked condition

- The VCO freq is proportional to the error voltage:

$$\omega_{osc} = \omega_o + K_0 V_e$$

- For the consistency of the analysis the VCO output should be expressed in phase rather than freq:

$$\phi_o(t) = \phi_o\Big|_{t=0} + \int_0^t \omega_{osc}(t)\,dt$$

- This integration permits to rewrite the VCO transfer function as:

$$\phi_o(s) = \frac{\omega_{osc}}{s} = \frac{K_0 V_e}{s}$$

- Using the classical linear feedback analysis the closed-loop transfer function is (ϕ_S is the phase of the input signal):

$$\frac{V_e}{\phi_s} = \frac{sK_D AF(s)}{s + K_D K_0 AF(s)}$$

PLL – in locked condition

- Defining the loop gain constant as: $K_L=K_DK_0A$, the closed loop transfer function is written as:

$$\frac{V_e}{\phi_s} = \frac{K_L}{K_0}\frac{sF(s)}{s + K_LF(s)}$$

- In practice we are interested in the input freq variation thus using:

$$\Delta\omega_s(s) = s\phi_s(s)$$

- The PLL transfer function in locked condition is is:

$$\frac{V_e}{\Delta\omega_s} = \frac{1}{s}\frac{V_e}{\phi_s} = \frac{K_L}{K_0}\frac{F(s)}{s + K_LF(s)}$$

- Typical loop filters have a low-pass transfer function

$$F(s) = \frac{1}{1 + s/\omega_1}$$

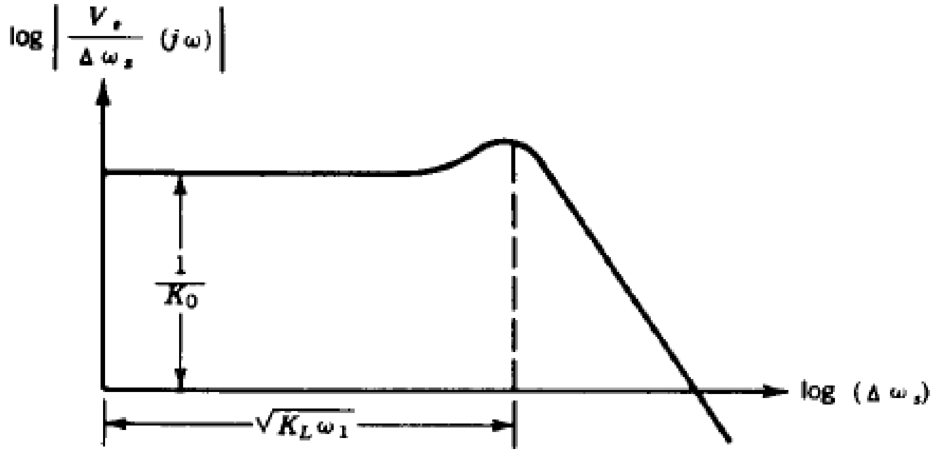
PLL – in locked condition

- The PLL transfer function can be thus rewritten as:

$$\frac{V_e}{\Delta\omega_s} = \frac{1}{K_0}\frac{1}{s^2/\omega_n^2 + (2\zeta/\omega_n)s + 1}$$

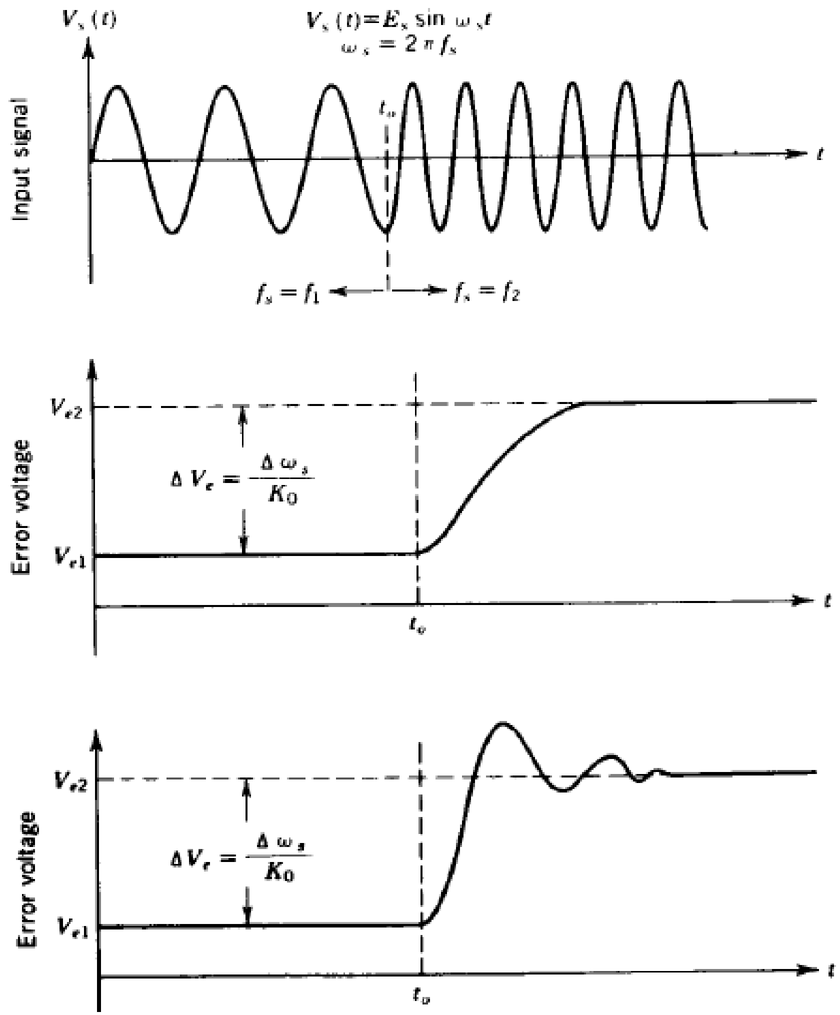
- where: $\omega_n = \sqrt{K_L\omega_1}$ $\quad \zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_L}}$

- The response in frequency is:



PLL – in locked condition

- Transient response of PLL to step change of input frequency



$\zeta > 1$

$\zeta < 1$

PLL – in locked condition

- In general the peaking in the frequency response is minimized, this corresponds to the condition $\zeta = 1/\sqrt{2}$, in this condition $\omega_1 = 2K_L$ and

$$\omega_{3\,\mathrm{dB}} = \omega_n = \sqrt{K_L \omega_1} = \sqrt{2}K_L$$

- In many application is required to have wide lock range (high K_L) and narrow bandwidth (low K_L), this is solved using the lag-lead filter as loop filter:

$$F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$$

- The damping factor is:

$$\zeta = \frac{1}{2}\sqrt{\omega_1/K_L} + \frac{1}{2}\frac{\sqrt{K_L \omega_1}}{\omega_2}$$

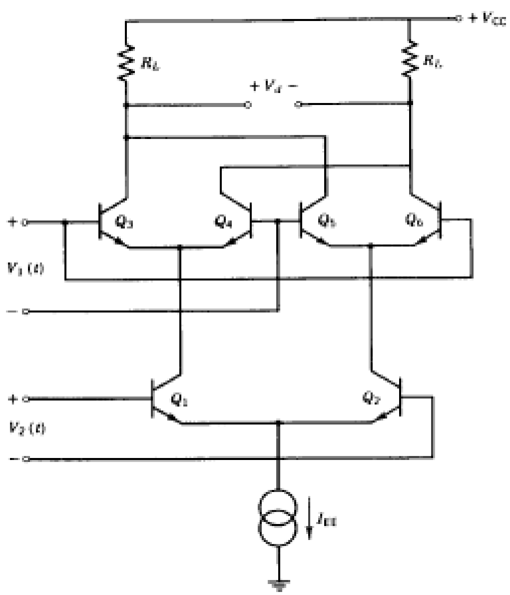
- Under the condition of maximally flat response, we have

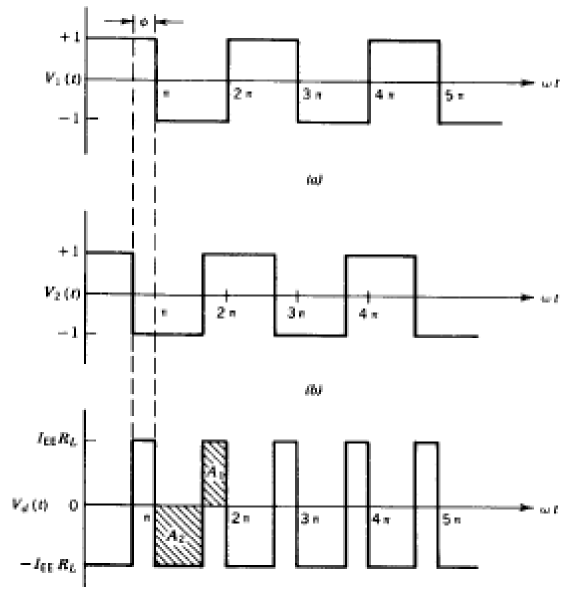
$$\omega_{3\,\mathrm{dB}} \approx 2\omega_n = 2\sqrt{K_L \omega_1}$$

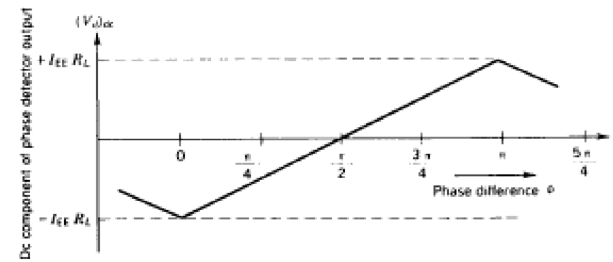
- Thus large loop gain and narrow loop bandwidth

PLL – lock range

- The maximum phase error which can be detected determined by the IC balanced modulator







- Thus $\pm(\phi_s)_{max} = \pm\frac{\pi}{2}$ rad and:

$$\Delta\omega_L = 2\pi\Delta f_L = \frac{\pi}{2}K_D A K_0 = \frac{\pi}{2}K_L$$

PLL – capture range

- Is the loop is open, at the output of the phase detector

$$V_d(t) = \frac{\pi}{2} K_D \quad \cos(\Delta\omega_i t)$$

- while at the output of the filter:

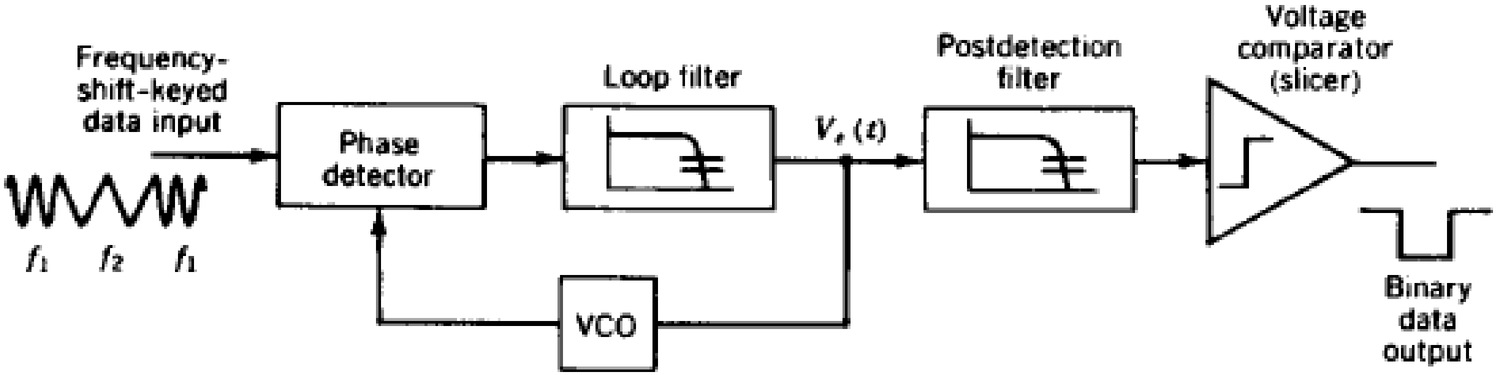
$$V_e(t)\Big|_{\text{peak}} = \frac{\pi}{2} K_D A \left| F(j\Delta\omega_i) \right|$$

- It is possible to demonstrate that

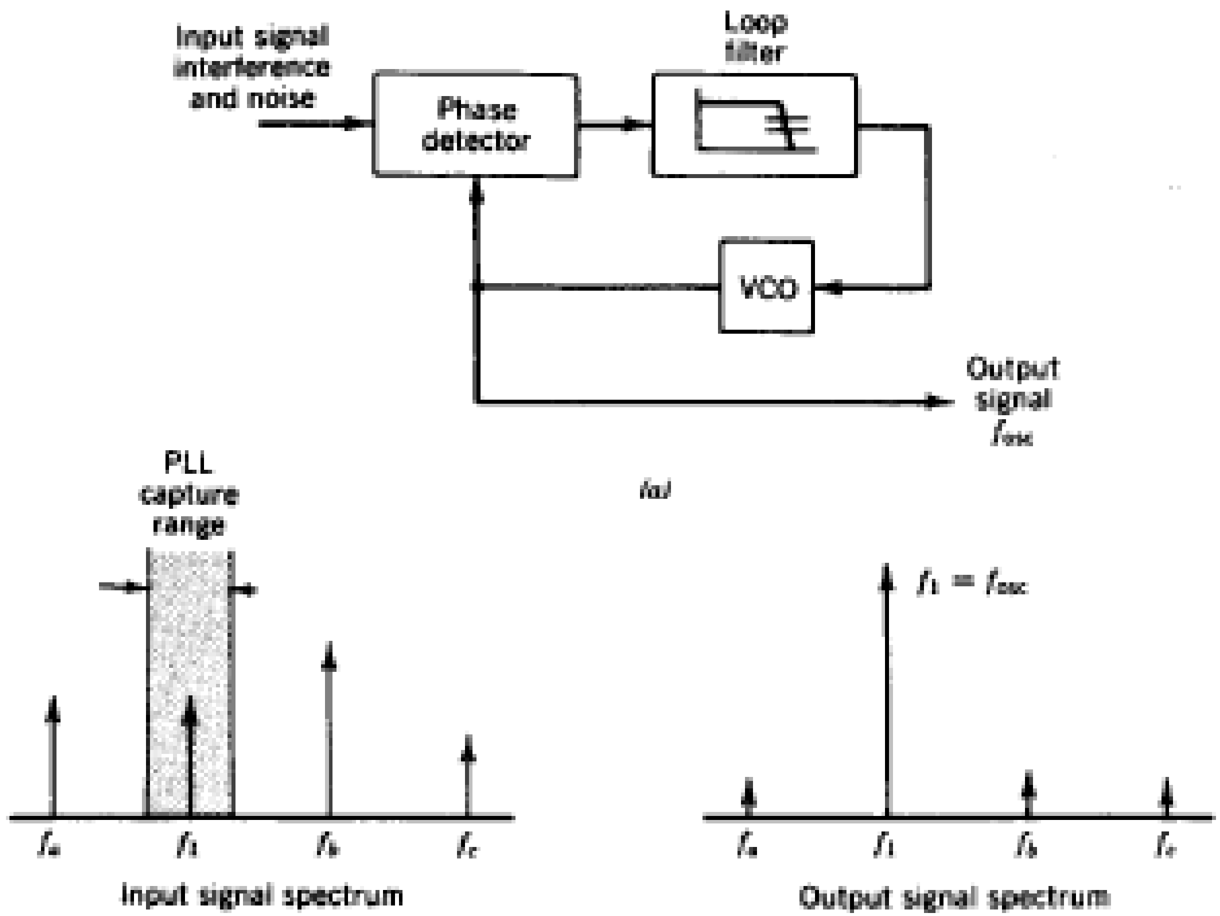
$$\Delta\omega_C\Big|_{\text{lag filter}} \approx \sqrt{\Delta\omega_L \omega_1} = \sqrt{\frac{\Delta\omega_L}{R_1 C_1}}$$

PLL application– frequency demodulation

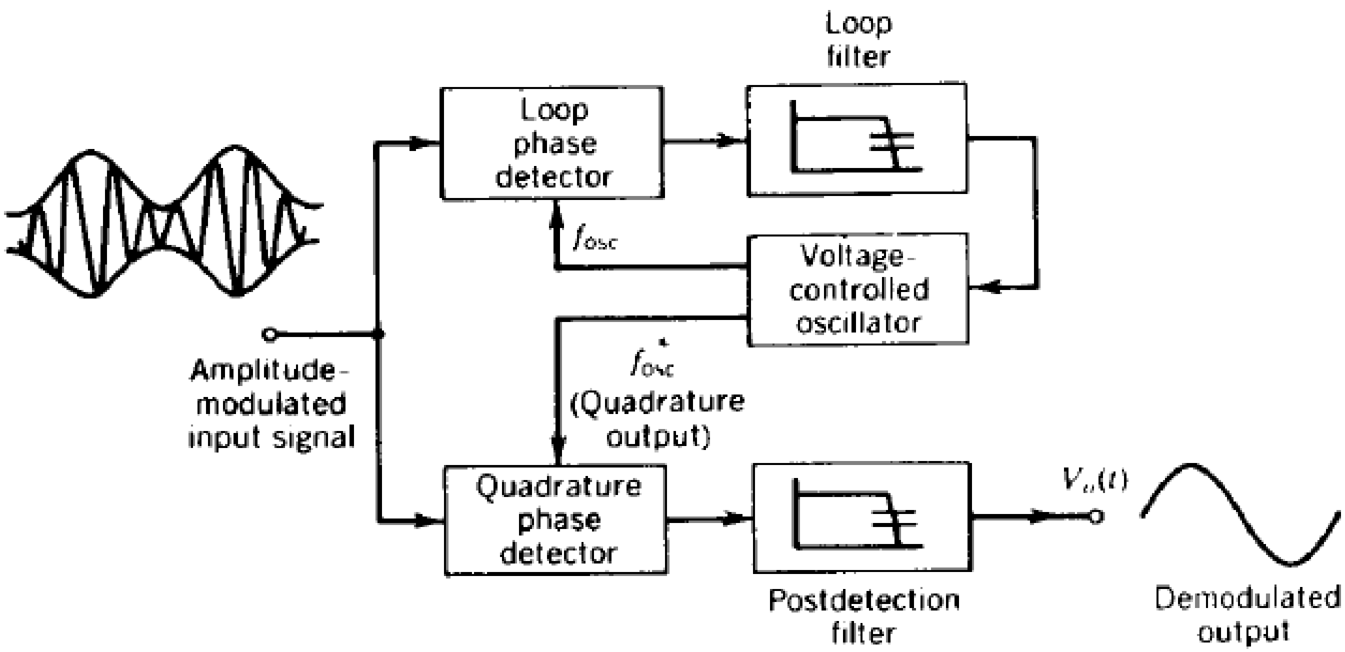
- FSK demodulator



PLL application– two carrier detection



PLL application– Synchronous AM detector



PLL application– local oscillator in transceiver