

Resonant Tunneling Devices: physics, technology and applications

Alessandro Cidronali

Dept. Electronics and Telecomm. Univ. of
Florence



Outline

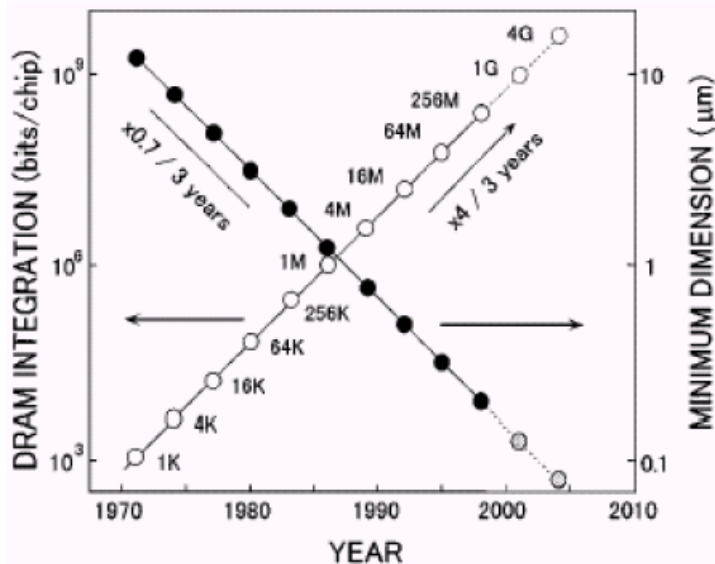
- motivations
- RTD basics
- RTDs physics and models
- Applications
 - ◆ Exploitation of the NDR
 - ◆ Digital applications (gate logic, memory)



Beyond the MOSFET

Moore's laws

- Integration has quadrupled every three year
- Minimum dimension has been scale by 0.7



- *Mesoscale* :
 - ♦ An intermediate scale, on the order of ~10 nm,
 - ♦ Materials have some properties of bulk material, but surface effects are important,
 - ♦ And more quantum phenomena become important
- *Bulk* :
 - ♦ Materials & structures fabricated using bulk processes with atomic precision
- *Electronics* :
 - ♦ Electron states are used for primary information-processing operations
 - not photons (optical), or whole atoms (mechanical)



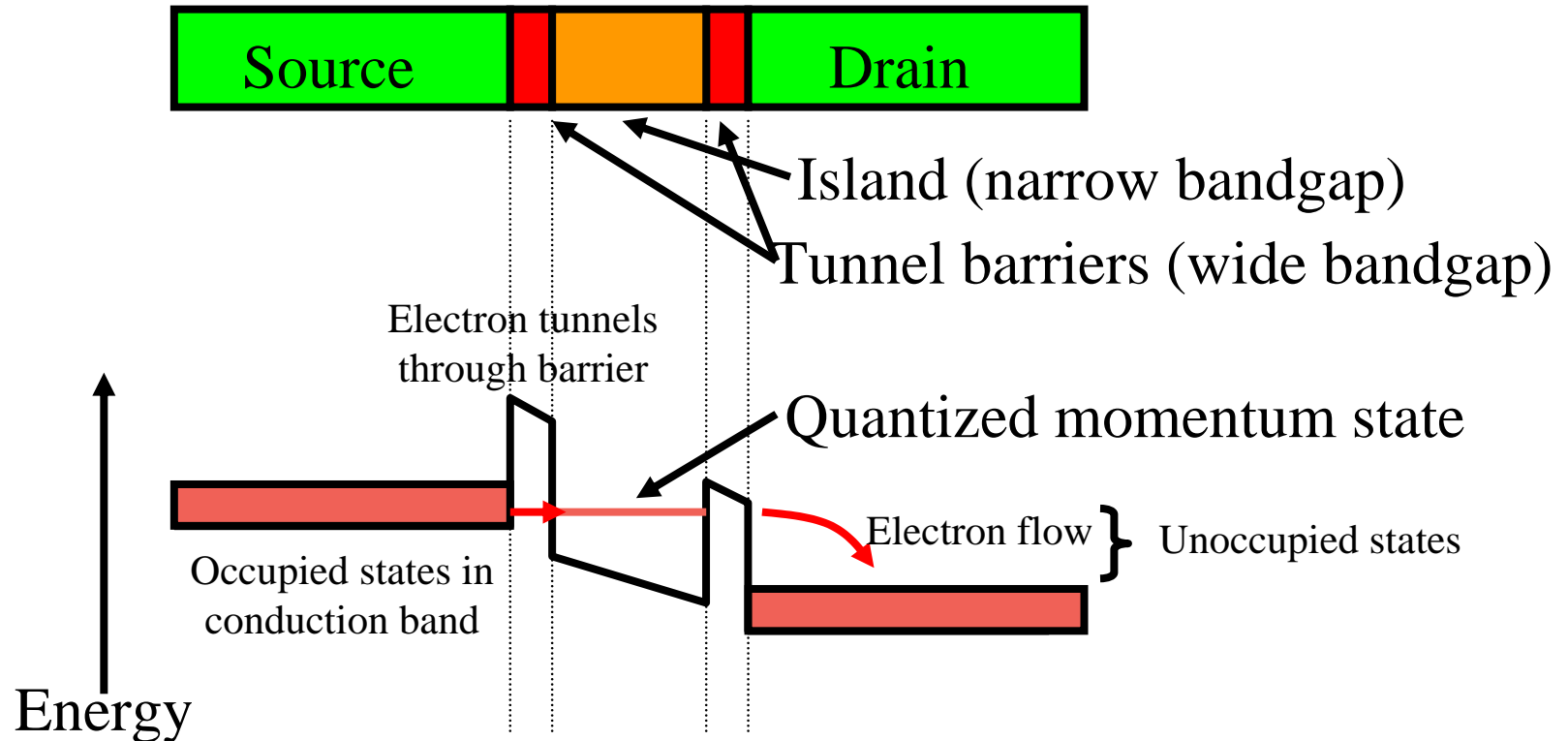
What happens @ mesoscale?

- MOSFET scaling hampered by quantization of:
 - ◆ charge:
 - becomes important @ $L \approx 10$ nm in all materials
 - ◆ energy levels:
 - important in semiconductors @ $L \approx 10$ nm
- Can alternative device operating principles *exploit* these quantization effects rather than be hampered by them?
- Some approaches:
 - ◆ Single-electron transistors
 - ◆ Quantum wells / wires / dots, quantum-dot CAs
 - ◆ **Resonant tunneling diodes / transistors**



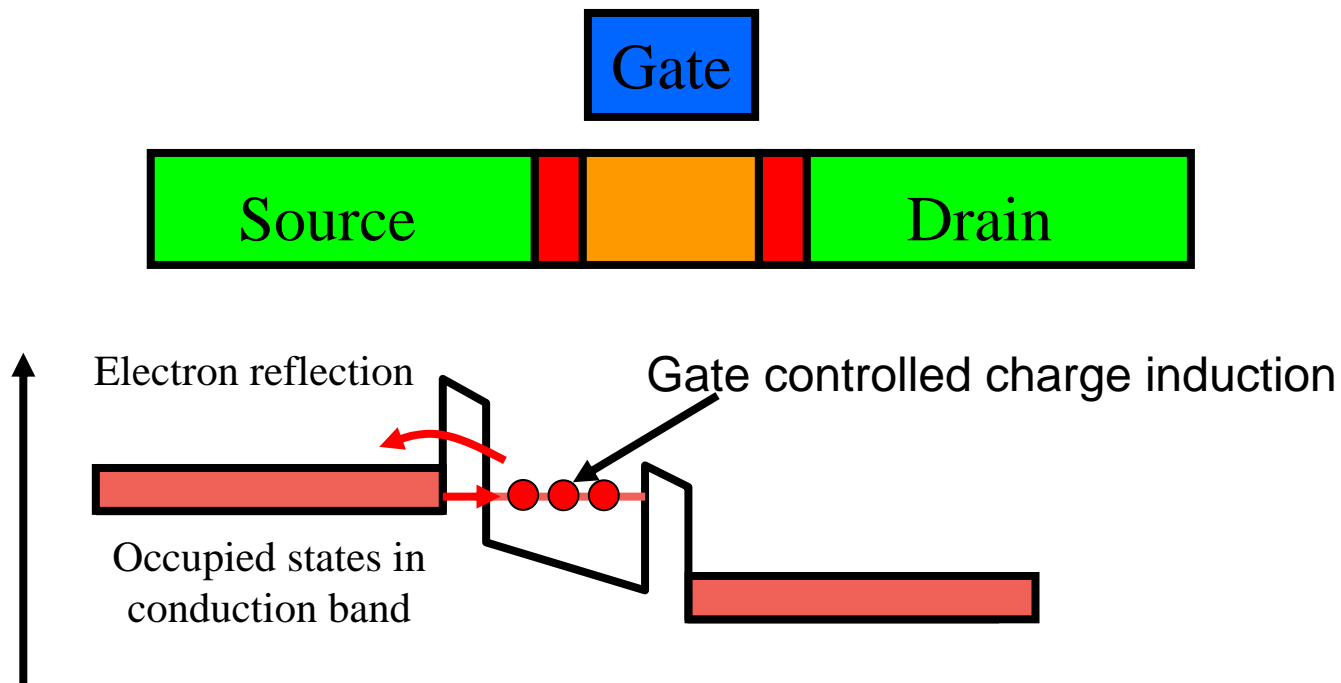
Resonant Tunneling Diodes

- Usually based on quantum wells or wires
 - ◆ 1-2 effectively “classical” degrees of freedom



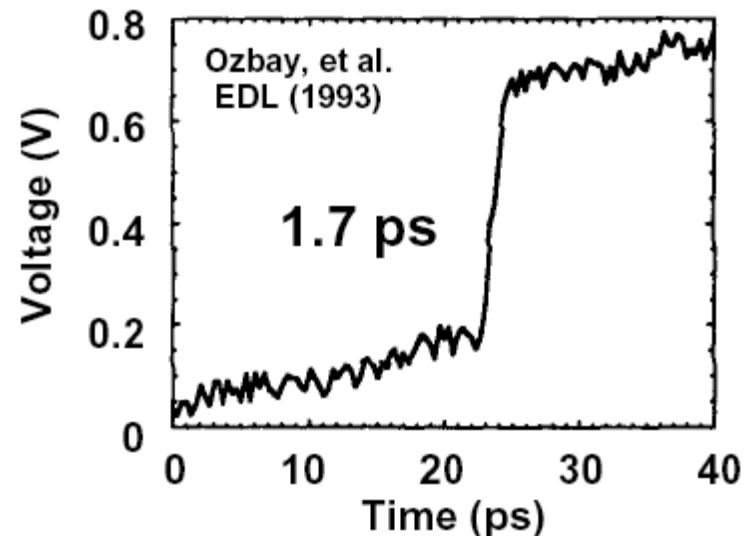
Resonant Tunneling Transistors

- Like RTDs, but an adjacent gate electrode helps adjust the energy levels in the island

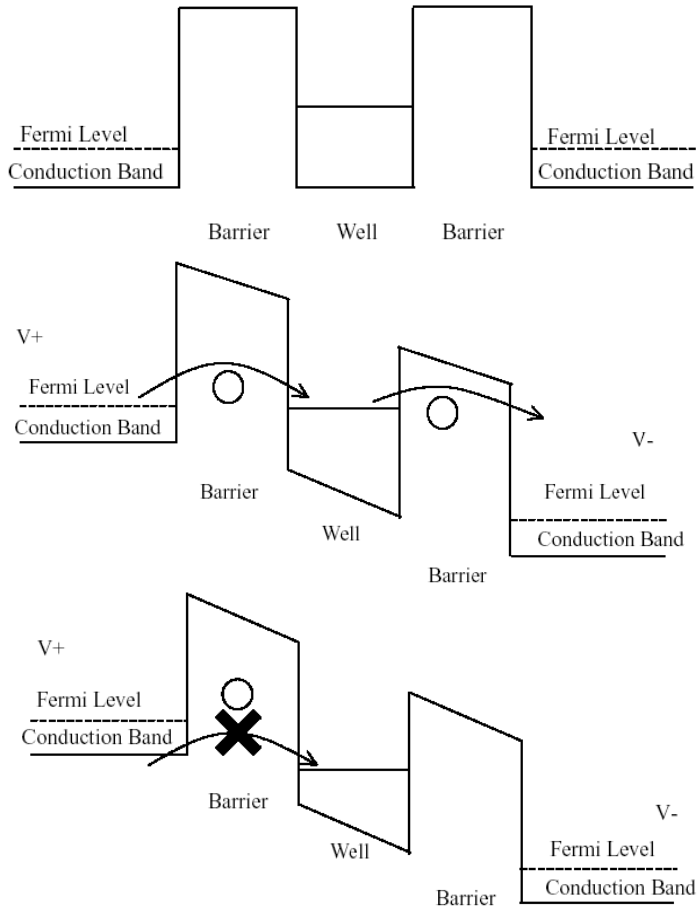


Why RTDs?

- Intrinsic bistability and high-speed switching capability (e.g., 1 ps switch, $f_{\max} \sim 1$ THz)
- Low power consumption
- Small device footprint
- Increased functionality

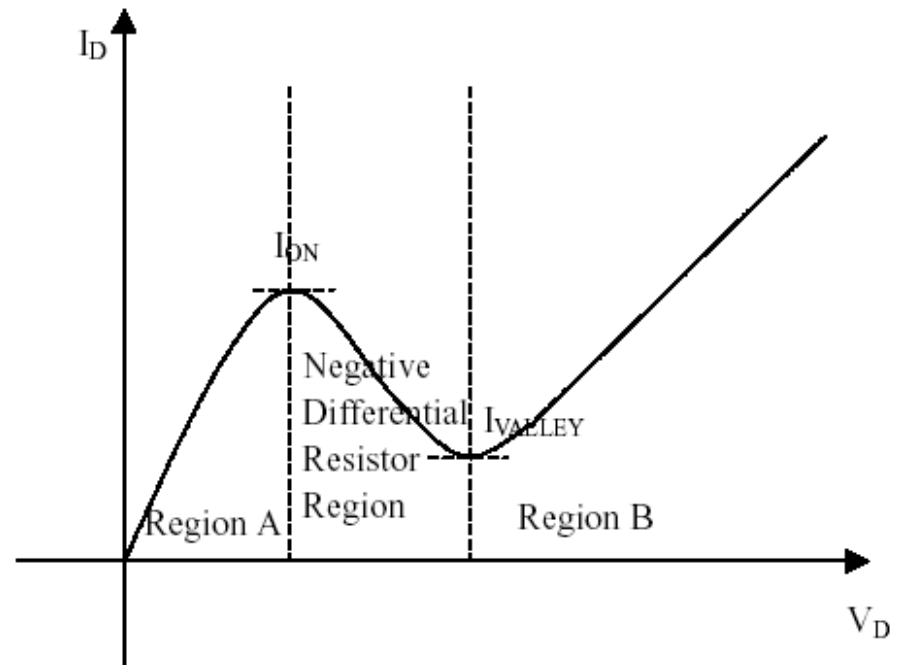


How does an RTD work?

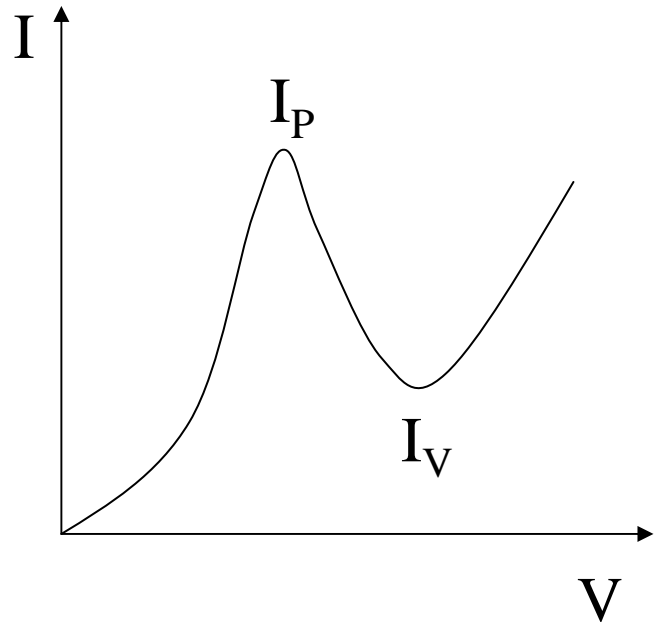


Peak current density: $I_P = I_{ON}$

Peak-to-valley current ratio (PVCR)
 $= I_{ON} / I_{VALLEY}$



Valley Current

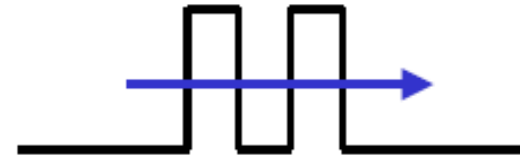


- ◆ Theory underestimates valley current because of:
 - (i) scattering by phonons and impurities
 - (ii) extra tunneling via impurity states in the barriers
 - (iii) tunneling via X and L states/bands
 - (iv) disorder in alloy barriers
 - (v) interface steps and roughness

Typical RTD structures

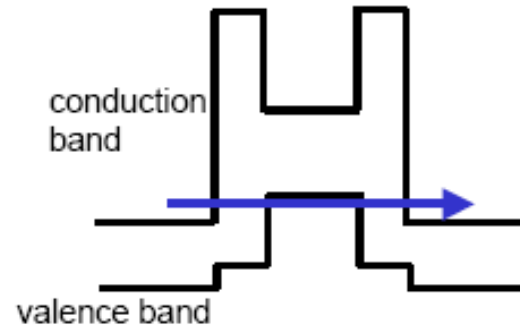
Intraband

GaAs/AlGaAs
GaAs/AlAs
InGaAs/InAlAs
Si/SiO
Si/SiGe

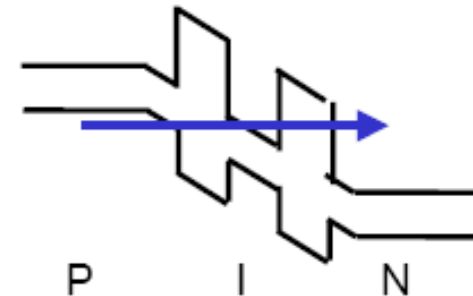


Interband

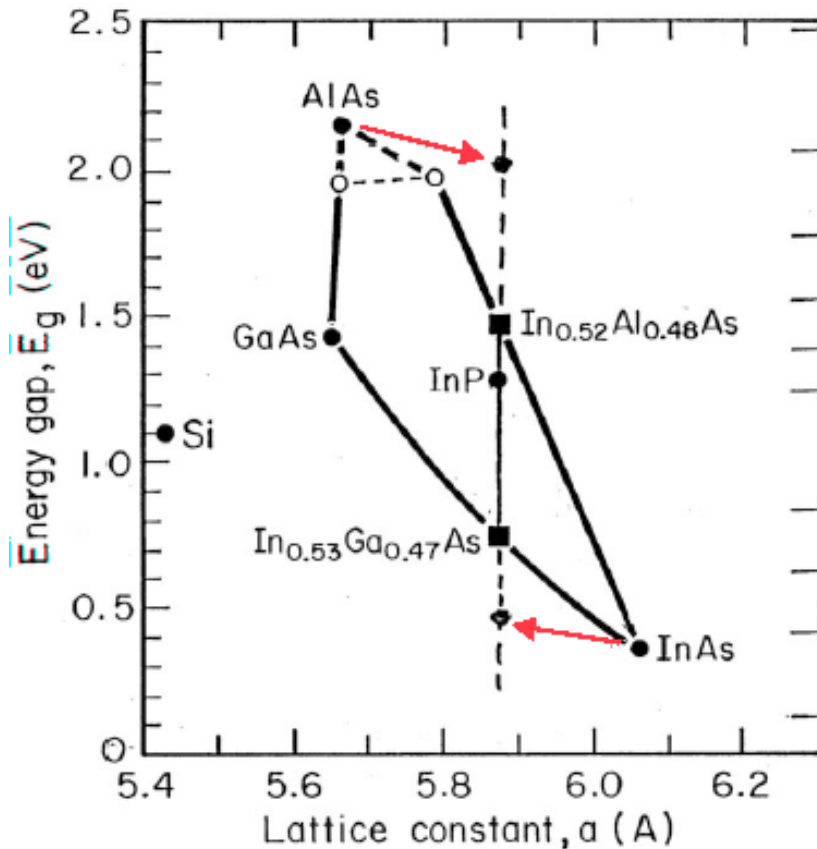
InAs/AlSb/GaSb



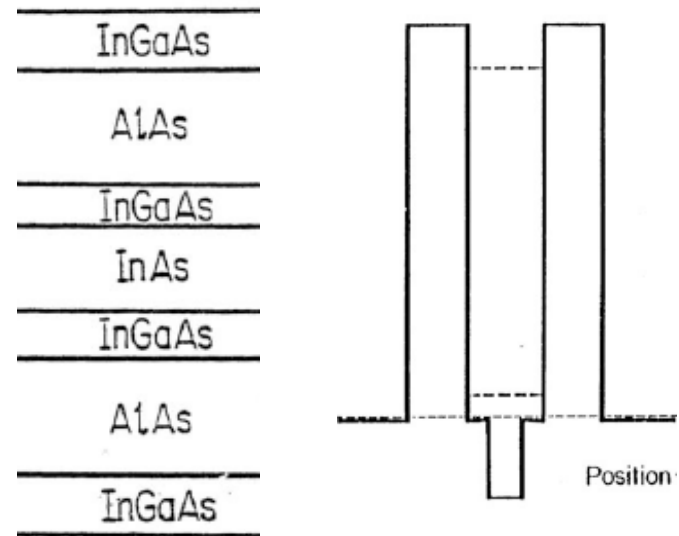
InGaAs/InAlAs (PIN diodes)



III-V RTDs

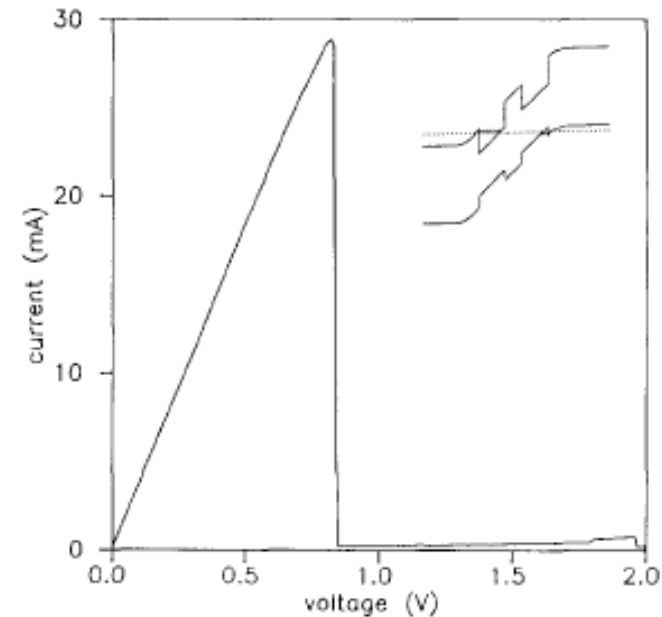
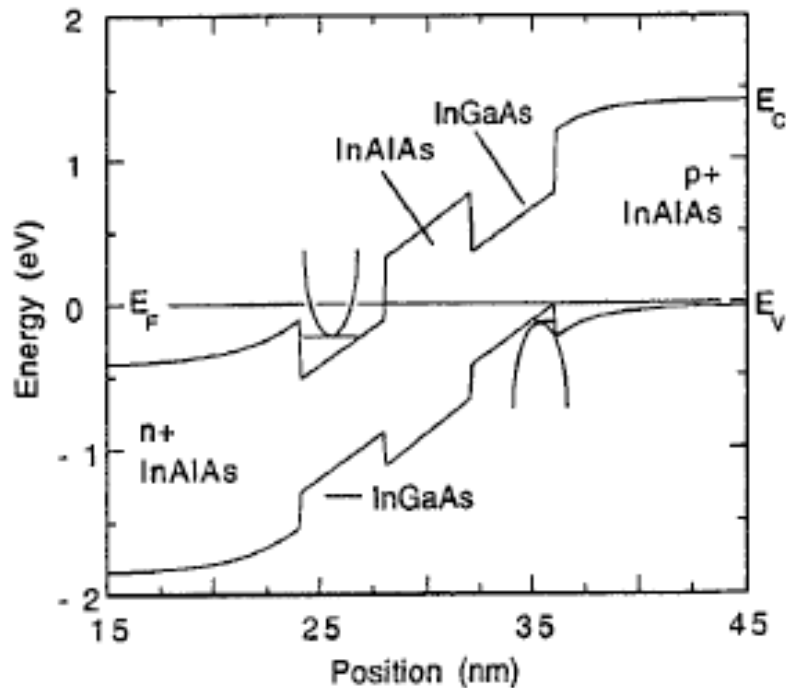


- GaAs family
 - ♦ AlGaAs/GaAs/AlGaAs
- InP family ($I_p=500$ kA/cm², PVC_R=52)
 - ♦ InGaAs/AlAs/InAs



RITDs

- p-n type I heterojunction double quantum well RITD



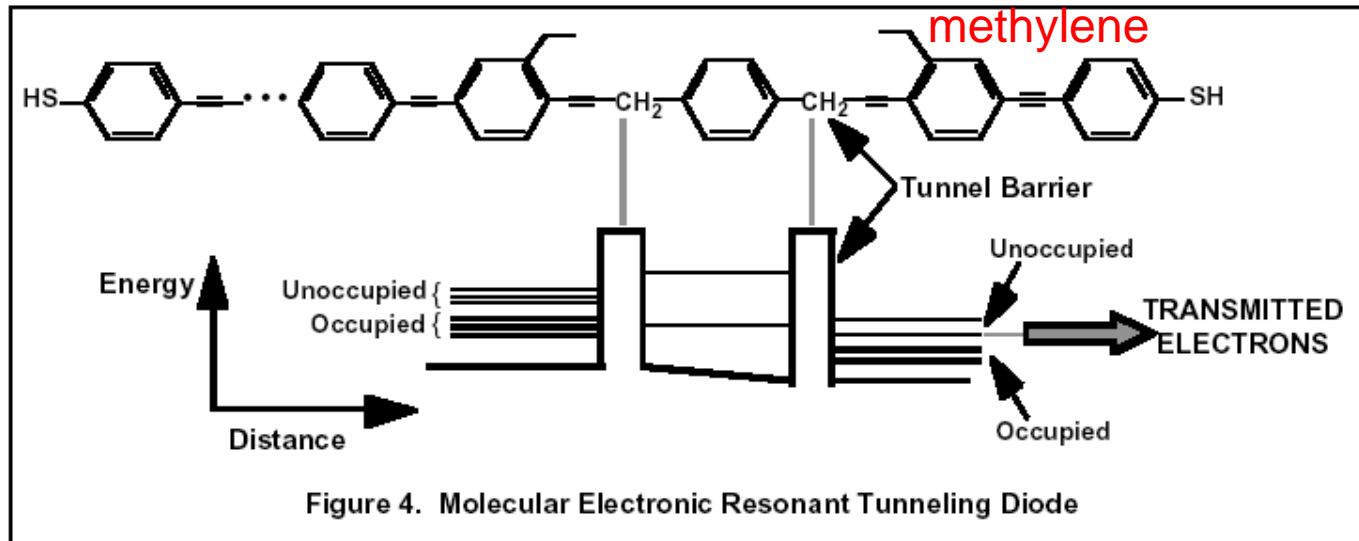
$$\text{PVCR} = 144$$

H. H. Tsai, et al., IEEE EDL, Vol. 15, no. 9, Sep. 1994



RTDs in other materials systems: Molecular RTDs

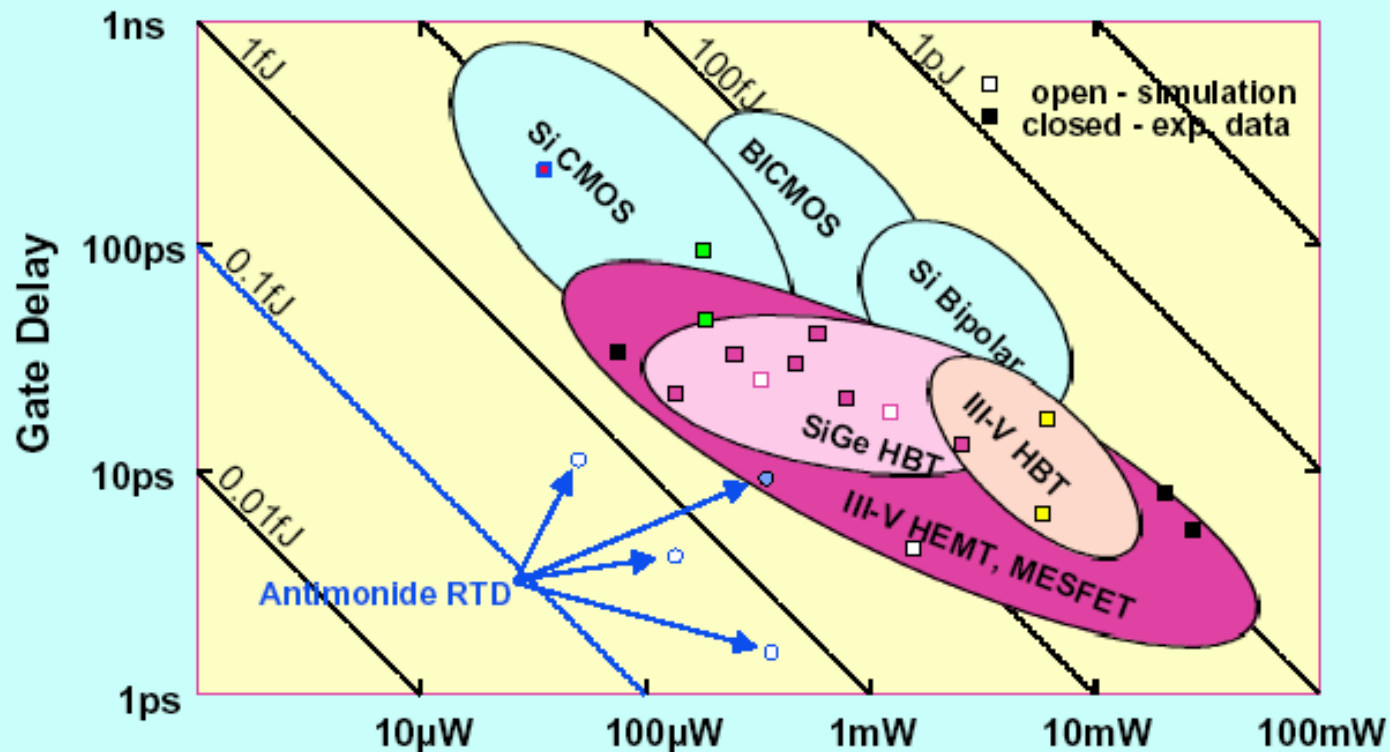
- Small (~1.5 nm): ultra-dense IC based on poly-phenylene
- Natural nanometer-scale structure: identical in vast quantities



James C. Ellenbogen, "A brief overview of nanoelectronic devices"



Power - Delay Product for Digital IC Technologies

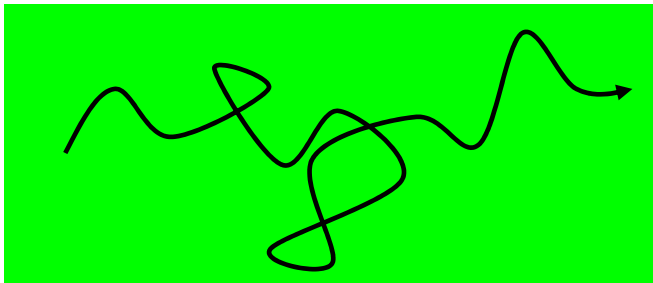


Power Dissipation

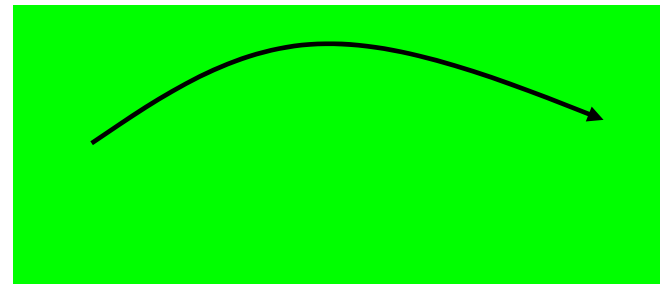
- data taken from U. König, et al., IEEE GaAs IC Symposium, pp14-18 (1995)
- Antimonide RTD data from W. Williamson et al., IEEE SSC **32**, 222(1997)
- Phillips, IEDM 95, p747; Siemens, op.cit. p739; NEC, IEDM 92, p. 397
- HRL, InP baseline and scaled process, 1997
- Vitesse FX and SCFX product data, GaAs MESFET, 1997
- Motorola, Complementary GaAs, GaAs IC Symp 95, p 18

Conventional Methods of Device Modeling

- Electrons are waves. de Broglie wavelength of an electron is:
$$h/p,$$
where p is the momentum
- Device dimensions are much larger than the electron wave length
- Transit time through the device is much larger than the scattering time
- Diffusion equation for semiconductors



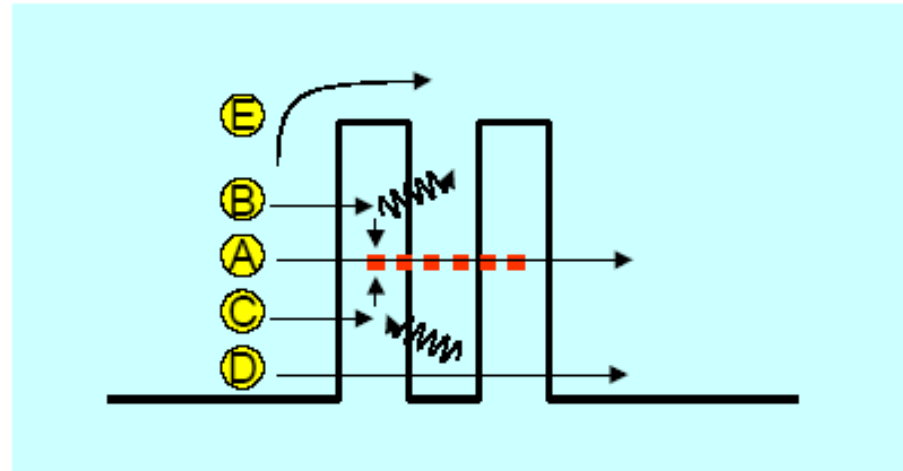
Diffusive



Ballistic

Phase-coherent

Transport processes in RTD

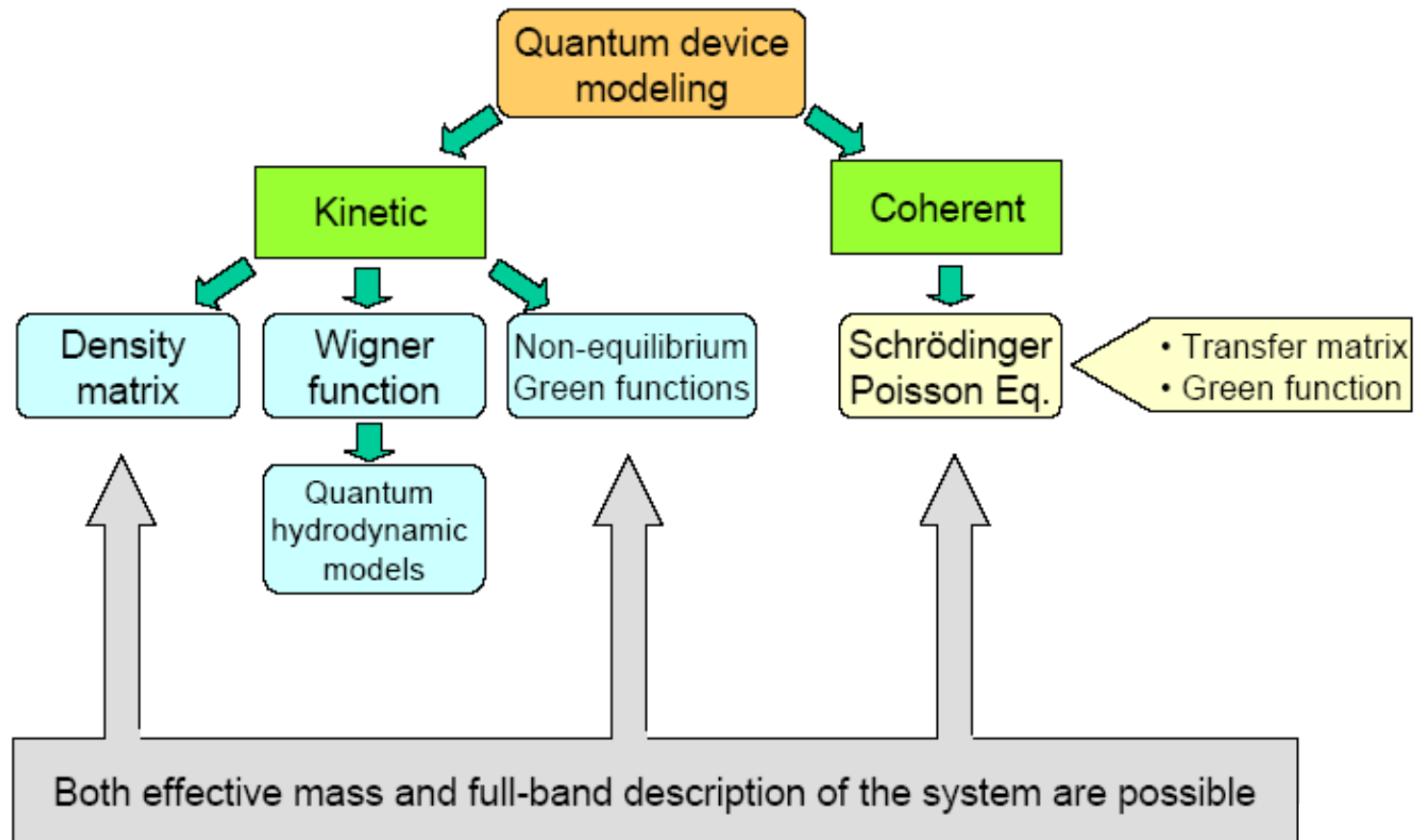


- A** Resonant tunneling
- B** Tunneling with phonon emission
- C** Tunneling with phonon absorption
- D** Non-resonant tunneling
- E** Thermionic emission

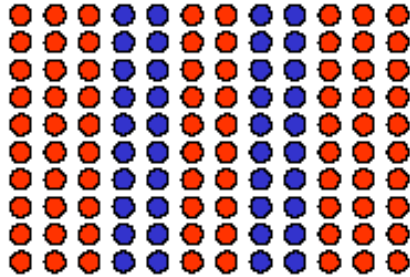
but also

- particle-particle interaction
- interface roughness
- impurities
- alloy disorder
- multi-valley tunneling

Quantum device modeling



coherent approach: Schroedinger eq.



$$H = -\frac{\hbar^2 \nabla^2}{2m} + V_{crystal}(\mathbf{r})$$

$$H\psi = E\psi \quad \text{Time independent Schrödinger Eq.}$$

Too complicated.... does exist any simpler approach ?

yes ! The **Envelope Function Approximation (EFA)**

In EFA the time independent Schrödinger Eq. reads:



$$\left[-\frac{\hbar^2}{2} \frac{d}{dz} \left(\frac{1}{m^*} \frac{d}{dz} \right) + V(z) \right] \varphi(z) = E\varphi(z)$$

m^* =effective mass

Boundary conditions !

The system is open since there is a current flux.

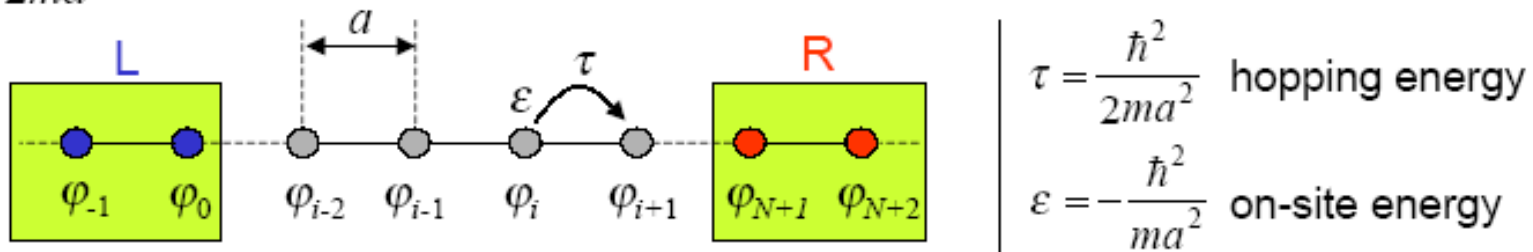
Usual boundary conditions, like infinite barrier or periodic repetition of the system, cannot be used.



Transfer Matrix: envelope function

Let us write the Schrödinger Eq. on a lattice (as you do to solve it numerically)

$$\frac{\hbar^2}{2ma^2}(\varphi_{i+1} + \varphi_{i-1} - 2\varphi_i) + V_i\varphi_i = E\varphi_i \quad \longrightarrow \quad \tau\varphi_{i+1} + \tau\varphi_{i-1} + (\varepsilon + V_i - E)\varphi_i = 0 \quad (1)$$



from Eq. (1)
$$\begin{pmatrix} \varphi_{i+1} \\ \varphi_i \end{pmatrix} = \begin{bmatrix} \frac{E - \varepsilon - V_i}{\tau} & -1 \\ 1 & 0 \end{bmatrix} \begin{pmatrix} \varphi_i \\ \varphi_{i-1} \end{pmatrix} = \Gamma_i \begin{pmatrix} \varphi_i \\ \varphi_{i-1} \end{pmatrix} = \Gamma_i \Gamma_{i-1} \begin{pmatrix} \varphi_{i-1} \\ \varphi_{i-2} \end{pmatrix} = \dots$$

If we define the transfer matrix $\Gamma = \prod_{i=1}^N \Gamma_i$ then
$$\begin{pmatrix} \varphi_{N+2} \\ \varphi_{N+1} \end{pmatrix} = \Gamma \begin{pmatrix} \varphi_0 \\ \varphi_{-1} \end{pmatrix}$$

Boundary conditions

In the left contact (L) $\varphi(x \in L) = e^{ikx} + re^{-ikx}$
 In the right contact (R) $\varphi(x \in R) = te^{ikx}$

$$\begin{pmatrix} te^{ik(N+2)a} \\ te^{ik(N+1)a} \end{pmatrix} = \Gamma \begin{pmatrix} 1+r \\ e^{-ika} + re^{ika} \end{pmatrix} \quad (2)$$



Tunneling current

The transmitted and reflected amplitudes, t and r , are obtained by solving the linear system in Eq. (2).

From the transmission amplitude t we can easily obtain the transmission coefficient T

$$T(E) = |t|^2 \frac{v_R}{v_L}$$

The tunneling current is

$$J = \frac{qm^*k_B T}{2\pi^2 \hbar^3} \int T(E) \log \left[\frac{1 + \exp((E_F - E)/k_B T)}{1 + \exp((E_F - E - qV_A)/k_B T)} \right] dE$$



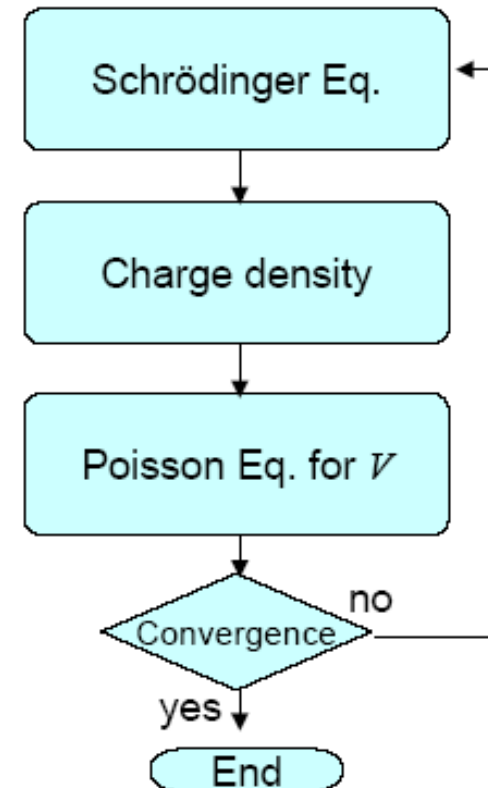
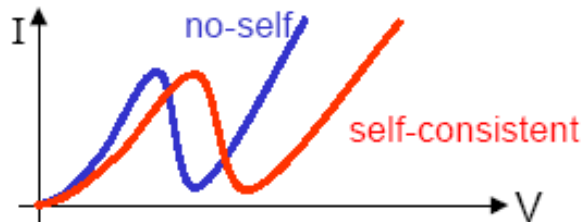
Self-consistent calculations

Fixed and free charge effects can modify via Coulomb interaction the band profile of the RTD. Coulomb interaction (Hartree level) is included self-consistently solving the Schrödinger and Poisson equation.

$$\left[-\frac{\hbar^2}{2} \frac{d}{dz} \cdot \left(\frac{1}{m^*} \frac{d}{dz} \right) + V(z) \right] \varphi(z) = E \varphi(z)$$

$$n(z) = \frac{m^* k_B T}{\pi \hbar^2} \sum_i |\varphi_i(z)|^2 \ln \left[1 + e^{\frac{E_F - E_i}{k_B T}} \right]$$

$$-\frac{d}{dz} \left(\varepsilon(z) \frac{d}{dz} V(z) \right) = q(N_D^+(z) - n(z))$$



Wigner function

$$i\hbar \frac{\partial}{\partial t} \psi(x,t) = \hat{H} \psi \quad \rightarrow \quad \rho(r,s,t) = \overline{\psi(r,t)} \cdot \psi(s,t)$$

Density matrix

1. Change of basis
2. Fourier transform

$$\frac{\partial f^W}{\partial t} + v \frac{\partial f^W}{\partial r} + \int dk' \Gamma(r, k - k') f^W(r, k') = \left(\frac{\partial f^W}{\partial t} \right)_{scat}$$

Wigner equation

$$\Gamma(r, k) = \frac{2}{h} \int_0^{\infty} dr' \sin(kr') [V(r + r'/2) - V(r - r'/2)]$$

V=potential

□ With the Wigner function it is easy to account for boundary conditions [Frensey '90]

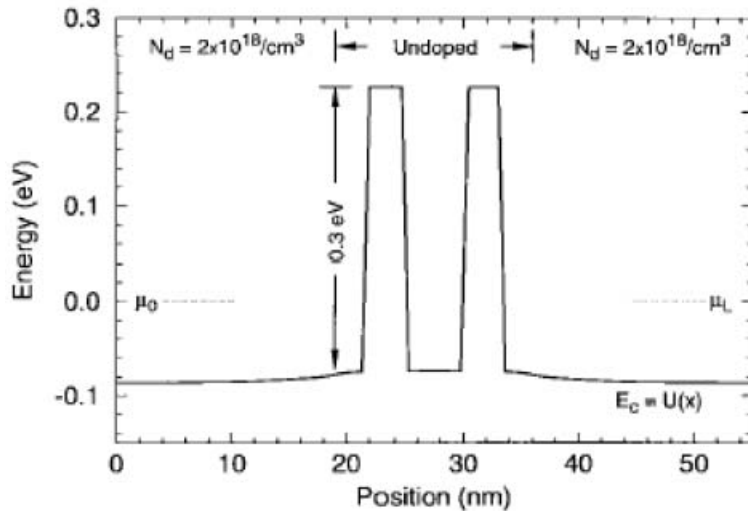
□ With the Wigner function it is difficult to define the collision term

$$n(r) = \int_{-\infty}^{+\infty} f^W(r, k) dk$$

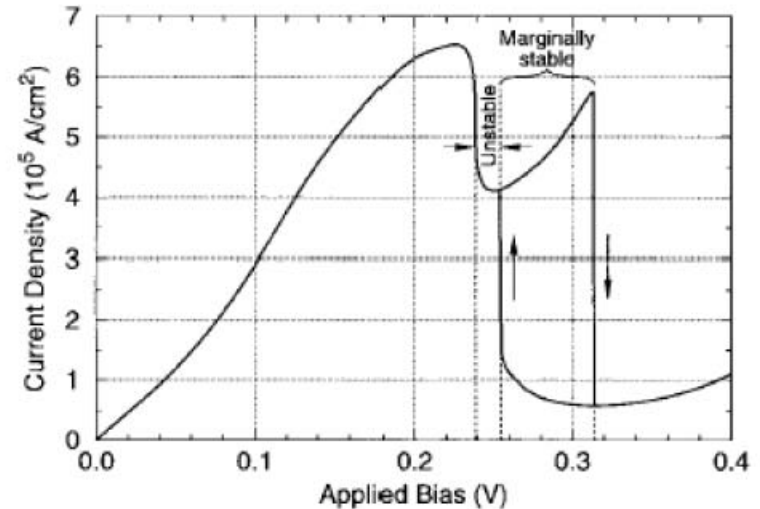
$$J(r) = -q \int_{-\infty}^{+\infty} k \cdot f^W(r, k) dk$$



Wigner function: results



Simulated GaAs RTD structure: equilibrium selfconsistent conduction band, Fermi levels, and doping. The 0.3 eV $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ tunnel barriers are 3 nm thick, and the GaAs quantum well width is 5 nm. The center 17 nm of the device (including 3 nm outside each tunnel barrier) are undoped.

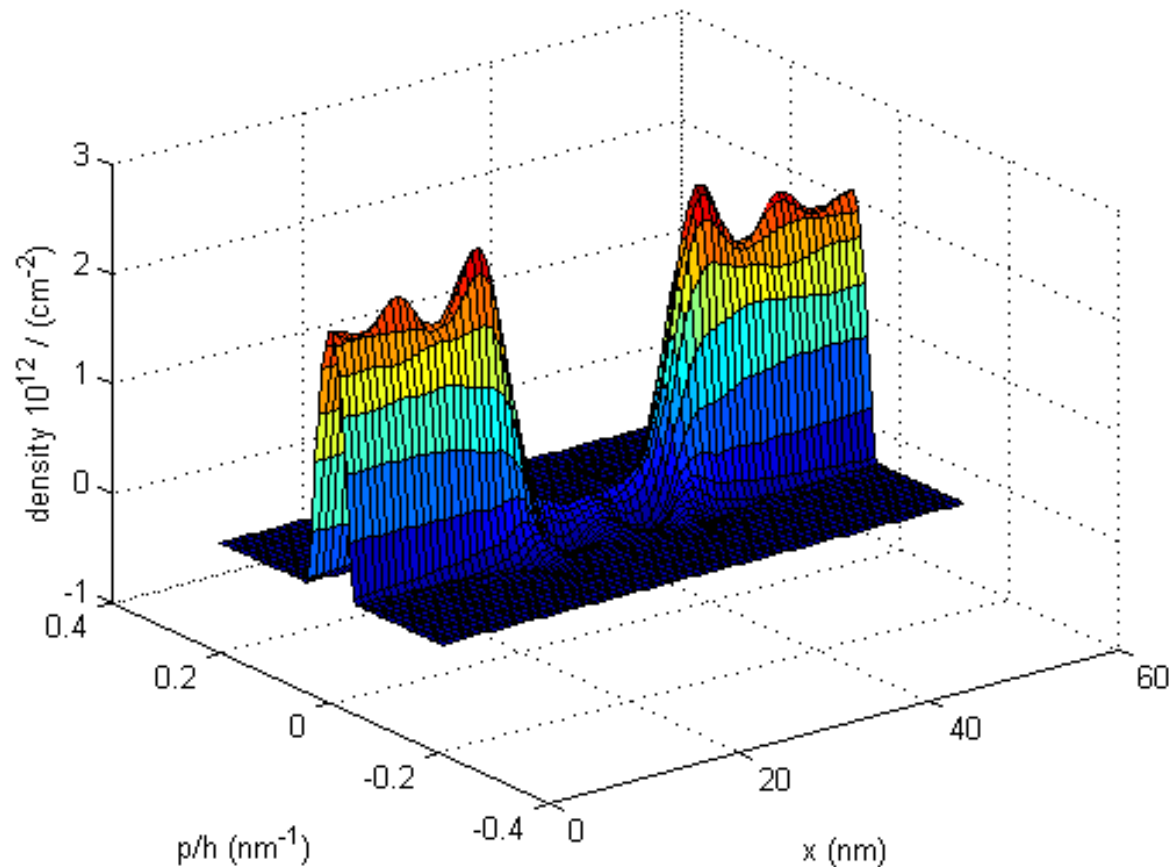


Self-consistent, steady-state RTD I-V curve showing negative differential resistance, hysteresis, and bistability. The RTD is unstable (oscillates perpetually) in the plateau between 0.239 V and 0.254 V, and it is marginally stable (oscillates with slow damping) in the remainder of the plateau.

Biegel and Plummer IEEE TED-44, 733 (1997)

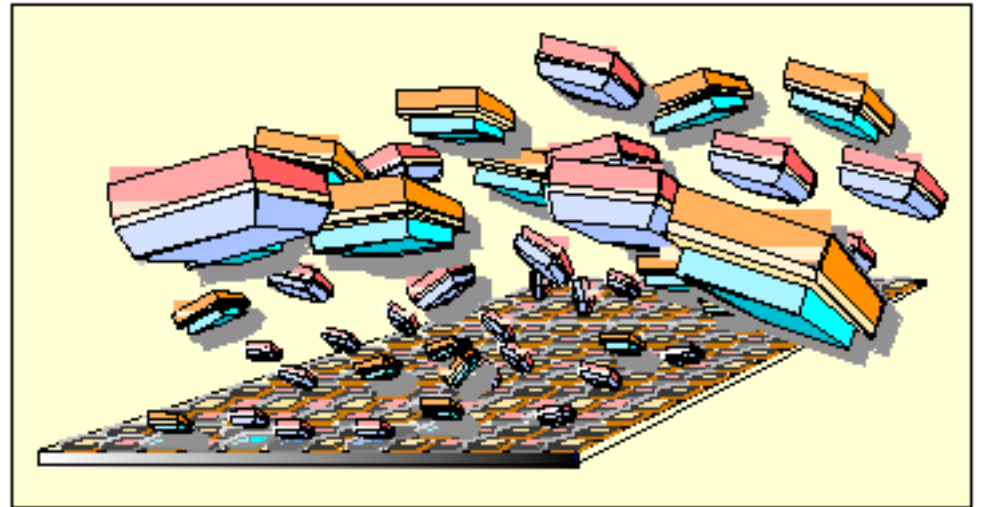
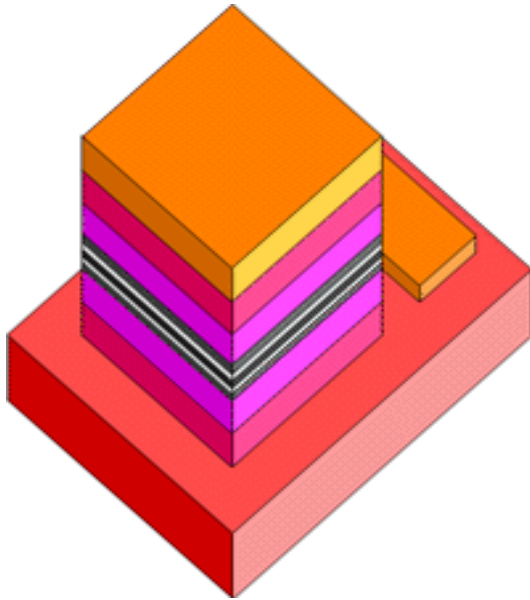


Wigner function: results



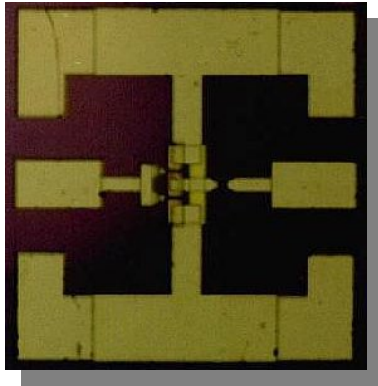
Applications

- Analog circuits ----- NDR & I²V square law
- Digital Logic ----- Bistability



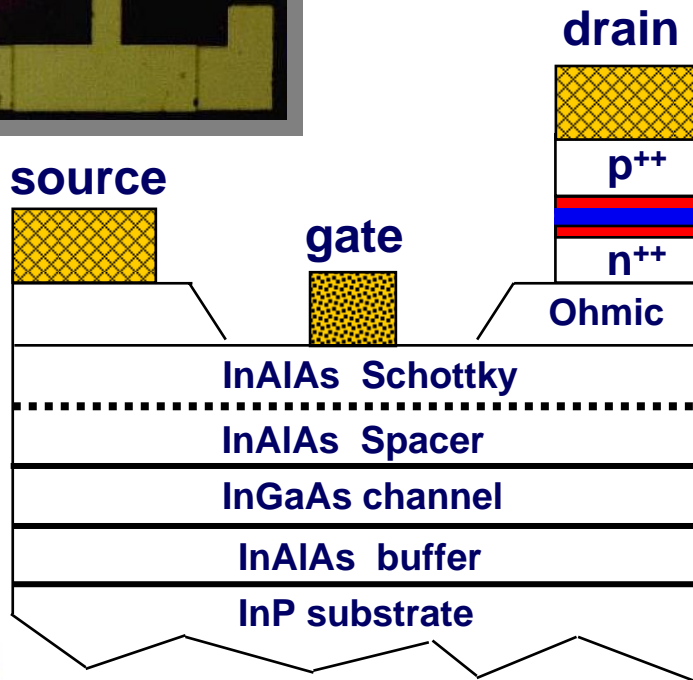
the HITFET structure for uW

Applications: QMMIC



better reliability

- ◆ HITD grown by MBE on top of HEMT layers
- ◆ improved Esaki diode (+1 well\1barrier): higher J_p/J_v and F_{max}
- ◆ because InP substrate, PVCR~50, F_{max} ~60GHz



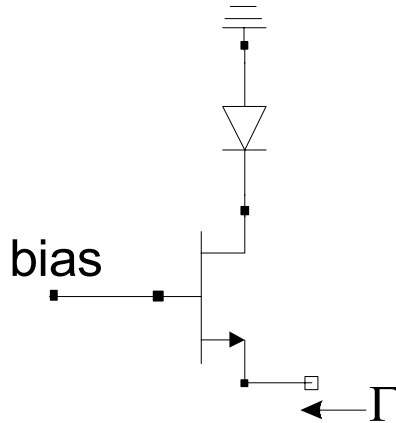
p ⁺ - InGaAs	Top contact layer (anode)	H I T D
n ^{id} - InAlAs	Barrier	
n ^{id} - InGaAs	Well	
n ⁺⁺ - InAlAs	Ohmic contact	
n ⁺ InGaAs	Bottom contact layer (catode)	H F E T
n ^{id} - InAlAs	Schottky contact (gate)	
n - InGaAs	Si δ -doping	
n ^{id} - InAlAs	Spacer	
n ^{id} - InGaAs	Channel	
n ^{id} - InAlAs	Buffer	
InP	Substrate	



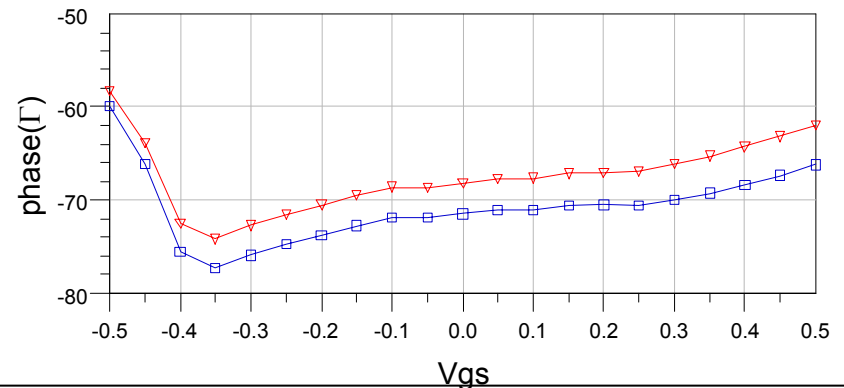
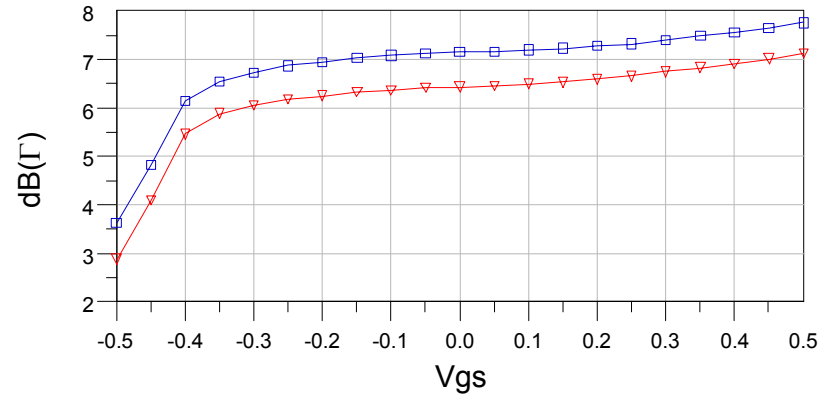
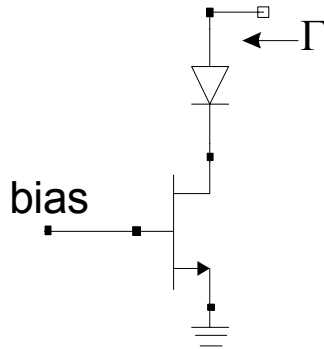
The drain-HITFET reflection coefficients

at 6.2GHz, $V_{\text{drain}} = 500\text{mV}$ as seen from the:

CD-HITFET

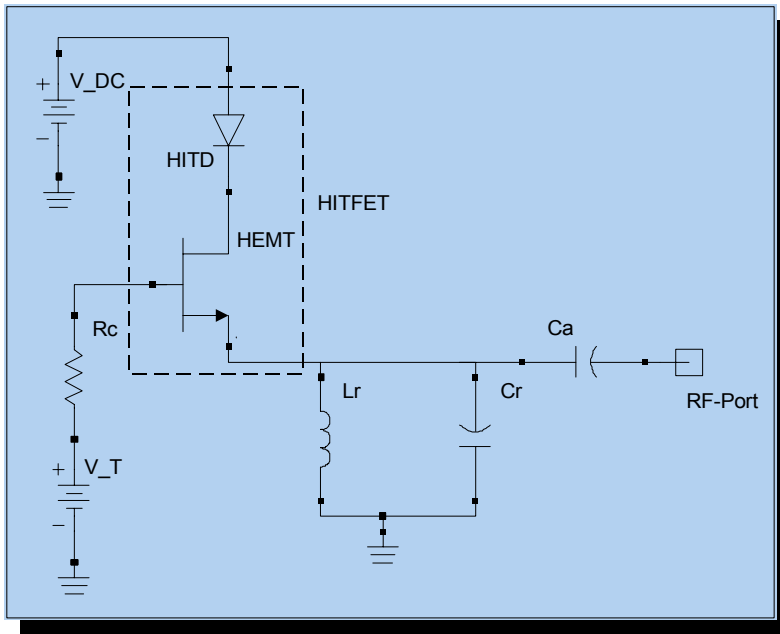


CS-HITFET

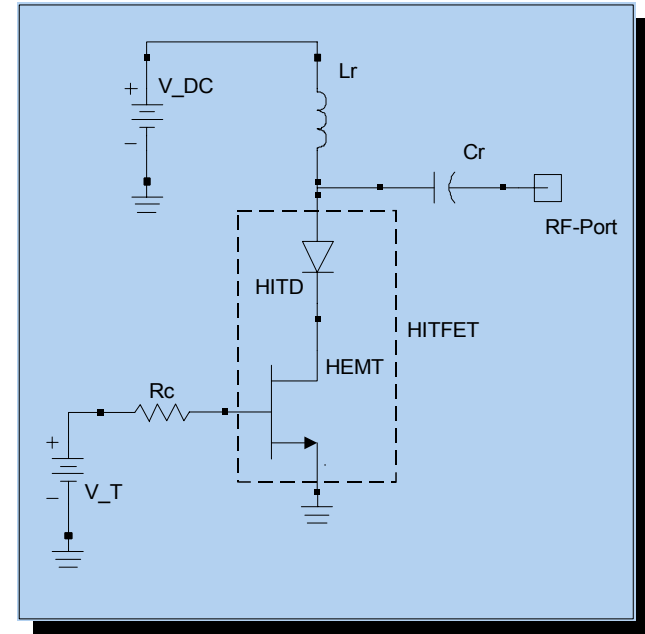


HITFET based VCO topologies/prototypes

Common-Drain (CD) VCO



Common-Source (CS) VCO



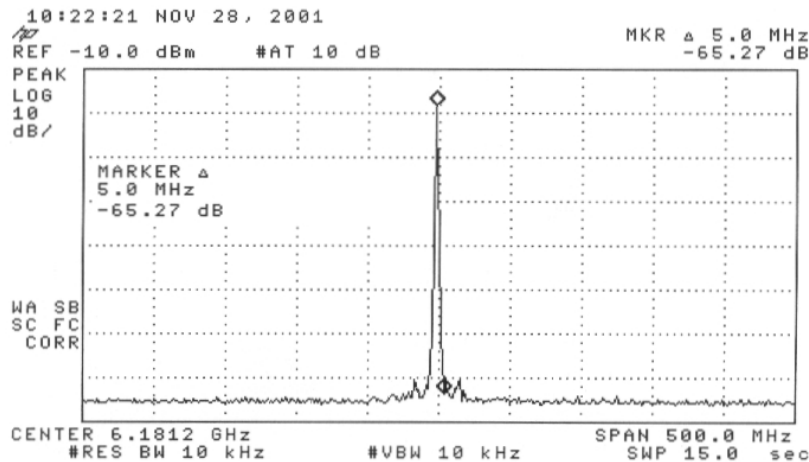
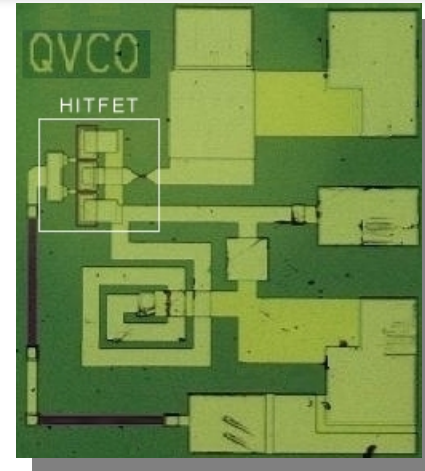
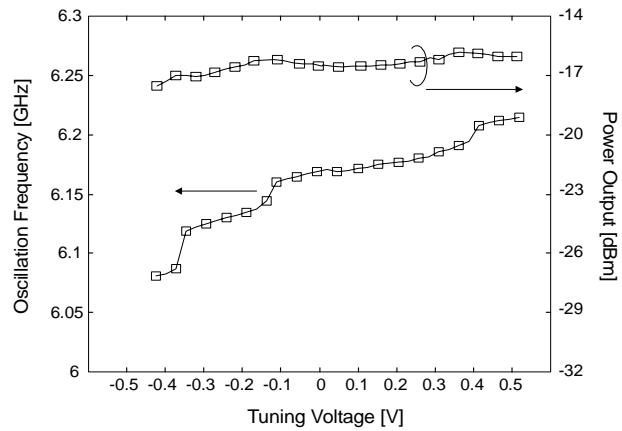
prototypes, all working at the bias voltage $V_{dc}=0.5V$:

'A' : CD-VCO @ 6.1GHz

'B' : CS-VCO @ 6.3GHz



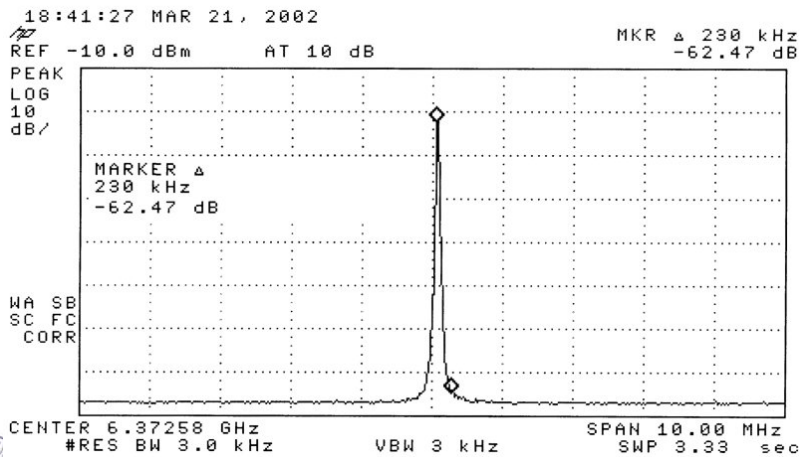
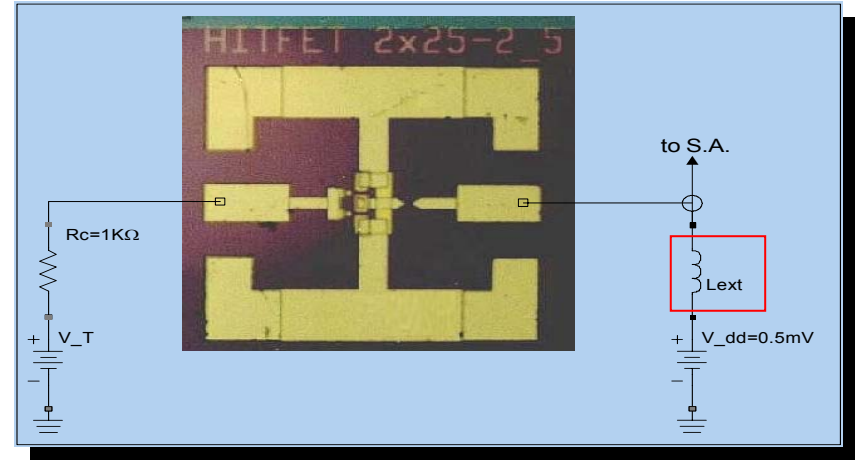
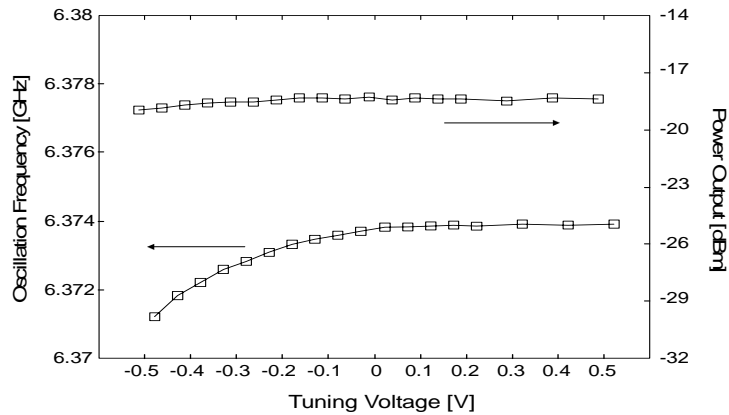
HITFET based VCO prototype 'A'



output frequency	6.18 GHz
output power	-16dBm
tuning range	140 MHz
SSCR	-105dBc/Hz @ 5MHz
efficiency	3%
power supply	850μW
supply voltage	500mV
die size	450x550μm ²



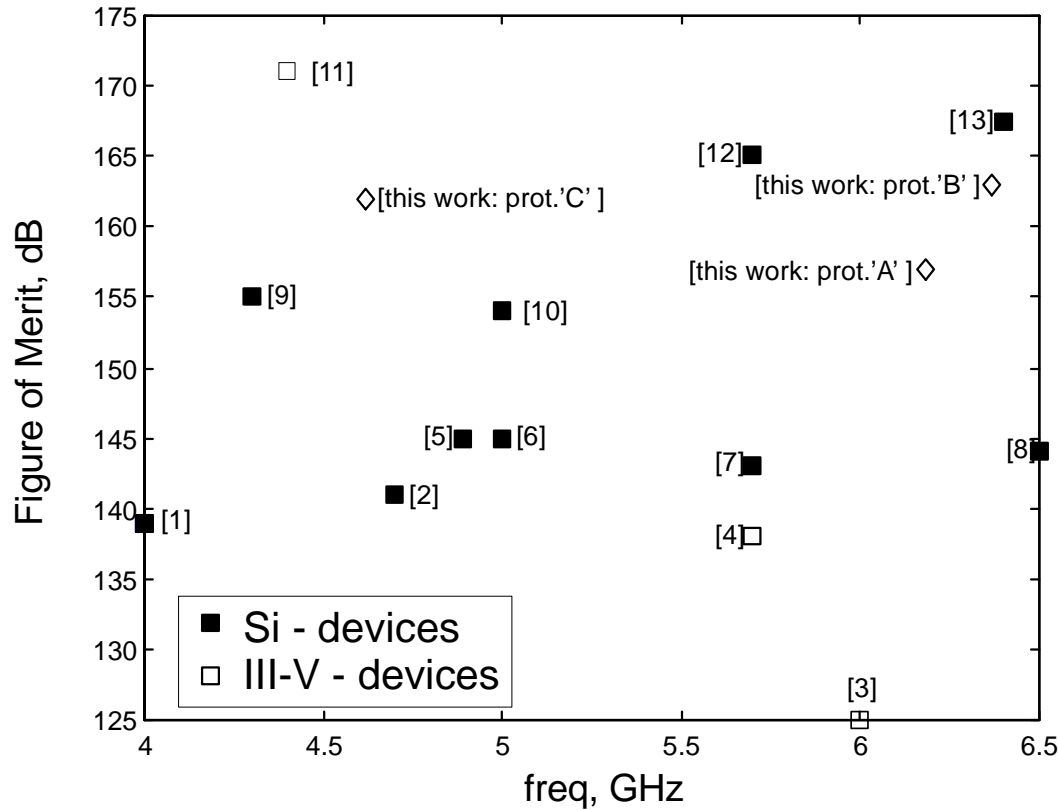
HITFET based VCO prototype 'B'



output frequency	6.37 GHz
output power	-17dBm
tuning range	3 MHz
SSCR	-97dBc/Hz @ 230KHz
efficiency	3%
power supply	850μW
supply voltage	500mV
die size	450x550μm ²



figure of merit (4-6.5GHz)



$$FOM = \left(\frac{f_0}{f_n} \right)^2 \frac{1}{P_{DC} \cdot SSCR(f_n)}$$

1. Arhens, **MOS w/ resonator**, proc. ISSC 1996
2. Kinget, **0.35um CMOS**, proc. ISSC 1998
3. Shealy, **GaN FET**, IEEE MWCL 2001
4. Yu, **InP HBT**, IEEE MWCL 2001
5. Mostafa, **0.35um CMOS sub-1V**, IEEE T-CS-II 2001
6. Mostafa, **0.35um CMOS**, proc. IEEE CS 2001
7. Loo, **BJT differential**, 2000 Canadian Conf.
8. Liu, **0.35um CMOS**, proc. ISSC 1998
9. Vaananen, **0.35um BiCMOS**, IEEE JSSC 2001
10. Van de Ven, **LC MOS**, 2001 Sym. VLSI
11. Ellinger, **classE GaAs VCO**, IEEE T-MTT 2001
12. Deval, **Synchronous CMOS VCO**, IEEE RFIC Sym. 2001
13. Klepser, **SiGe BiCMOS**, IEEE RFIC Sym. 2001

HITFET-VCOs show the lowest power supply



the QMMIC limitation

- **Not all the active functions can be replaced; e.g. difficult to replace LNA, PA, Switch**
- **On a one-to-one basis, the individual functions in QMMIC could be more effective than conventional ones (e.g. VCOs and mixers)**
- **In the overall budget, however, the benefit might be marginal**



the QMMIC as enabling technology

- ◆ How to improve the effectiveness taking advantage of the unique features of QMMIC technology?
- ◆ By introducing appropriate architectures whose application is enabled by the features of QMMIC technology

- enabling technology approach -

the Quantum Bi-Directional Amplifier (QBDA) for

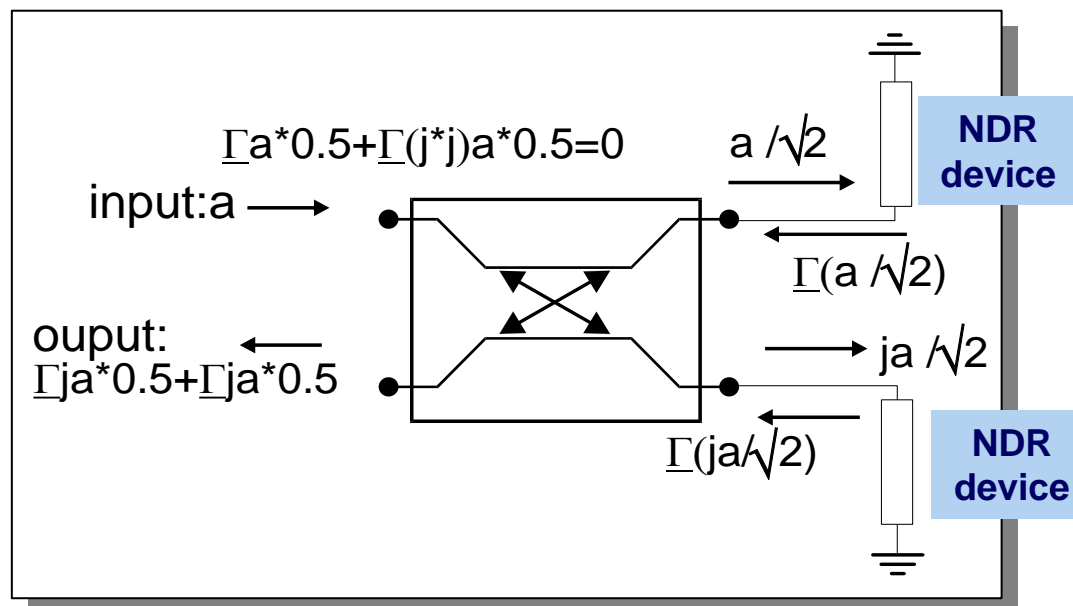
Tagging Applications



Bi-directional amplifier based on HITD

The basic idea:

- ◆ The reflection coefficient (Γ) of a device exhibiting a NDR is >1
- ◆ Combining by a 90° directional coupler two HITDs, the output signal is Γ times the input one



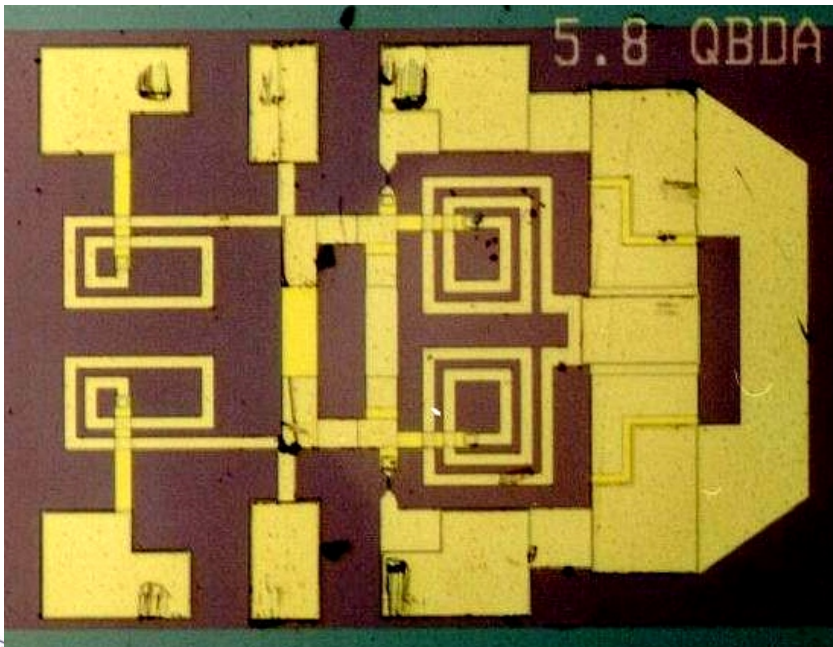
The scattering matrix is of the form:

$$S = \begin{vmatrix} S_r & S_t \\ S_t & S_r \end{vmatrix}$$

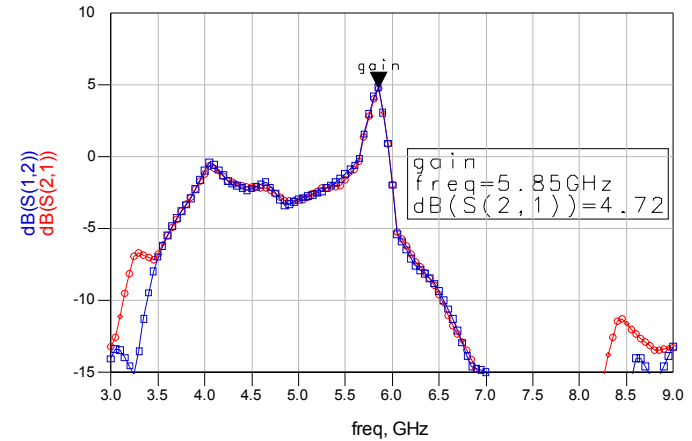


QBDA prototype

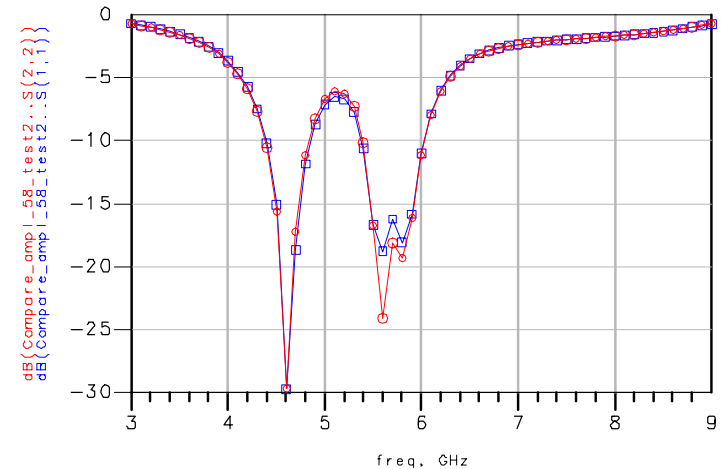
- A Quantum MMIC bi-directional amplifier has been demonstrated @ 5.8GHz; main characteristics: 450mV\0.5mA power supply, gain 4.7dB. More work to control the HITD parameters is required.



dB(S12), dB (S21)

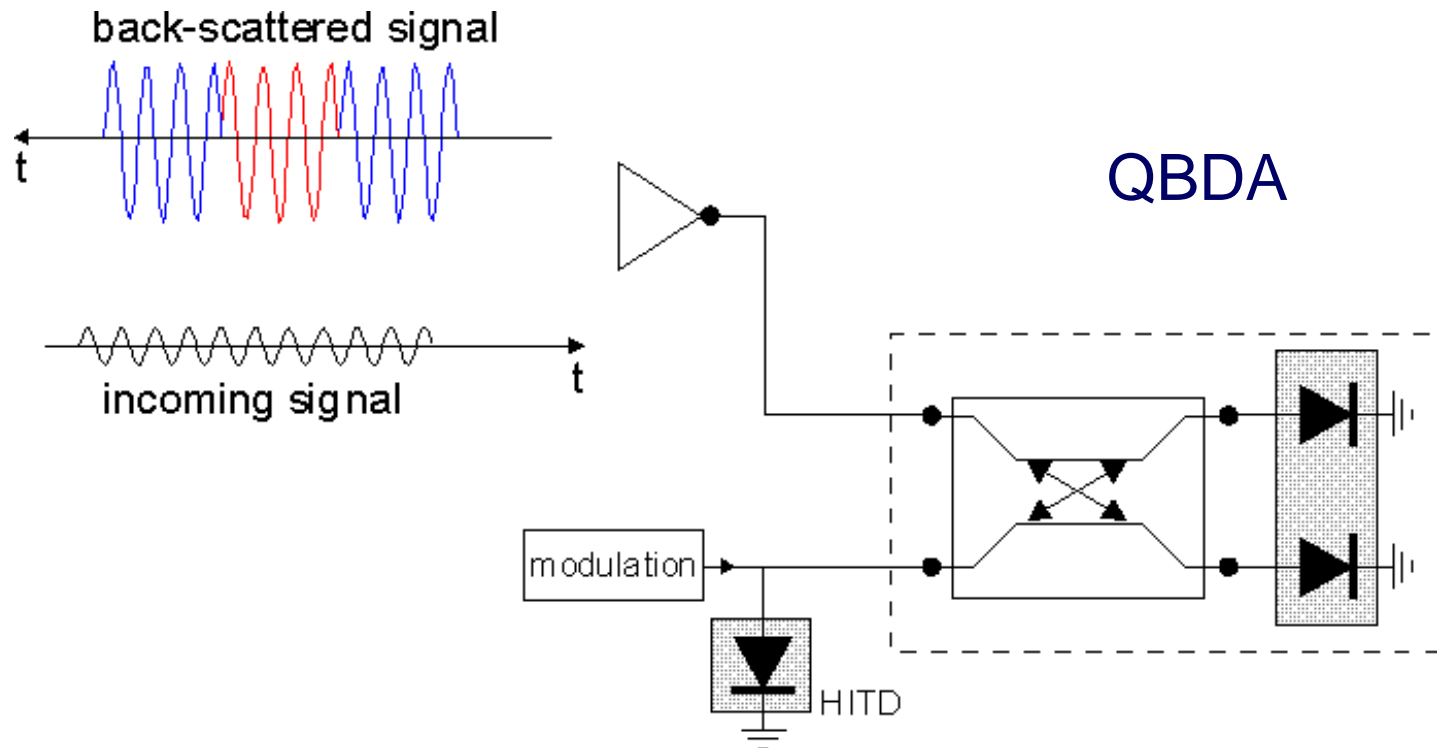


dB(S11), dB (S22)



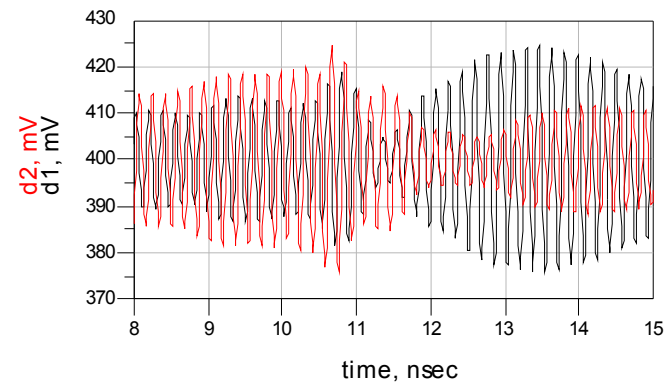
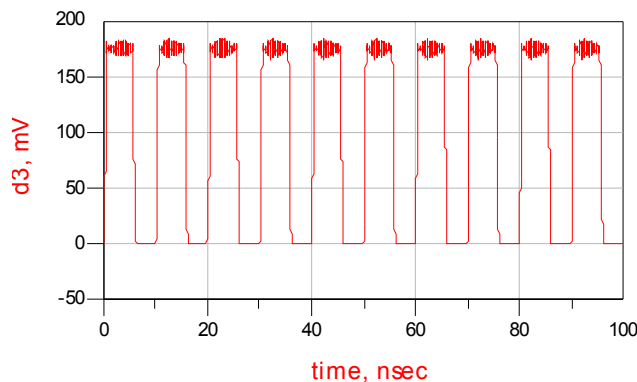
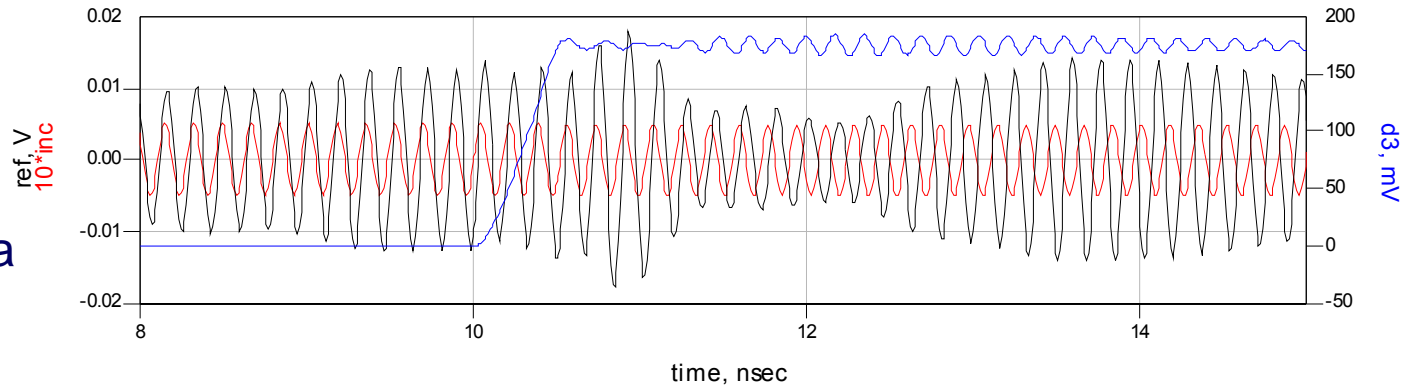
An application of the QBDA: the PM reflective TAG

Terminating a port of the QBDA by a two-state load (e.g. a HITD properly biased) a reflection equal to 2 times the QBDA gain is obtained with a phase swing of 180°



An application of the QBDA: the PM reflective TAG

Terminating a port of the QBDA by a two-state load (e.g. a HITD properly biased) a reflection equal to 2 times the QBDA gain is obtained with a phase swing of 180°



QMMIC Summary

◆ Highlights:

- TDs may be considered as an *optimizing* technology for extremely low power (<500mV) RF electronics, (e.g. VCO).
- new circuit functionalities are *enabled* by Tunnel Devices.
- at system and circuit levels, TDs introduce new degree of freedom, (e.g. BDA).

◆ Next steps:

- Tight control of series resistance and parasitics.
- Device engineering at quantum mechanic level.
- Application to millimeter-wave transceiver

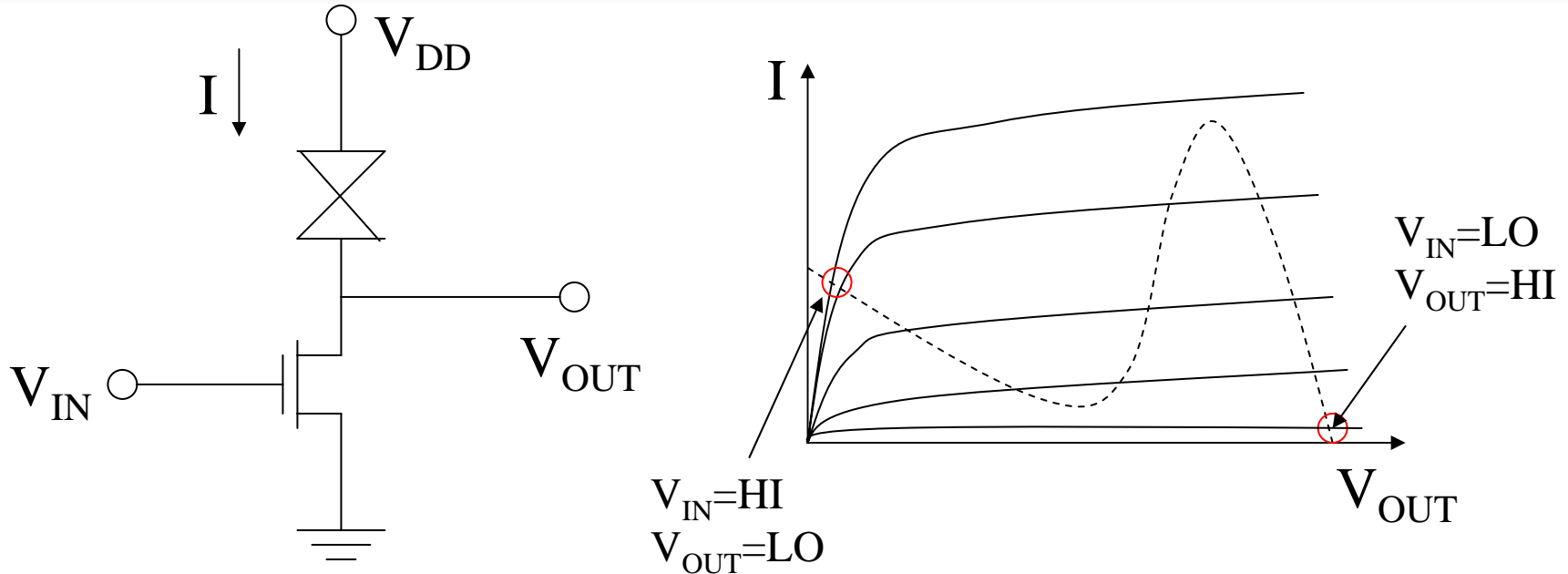


Applications — Digital Logic

- Logic circuits ----- Bistability
- Integration with transistors (HEMT, HBT, CMOS) is a requirement for a complete IC technology based on RTDs
 - ◆ Transistors: Input/output isolation, controllable gain
 - ◆ RTDs: increased functionality, enhanced circuit speed, reduced power consumption
- It's all about Load lines!

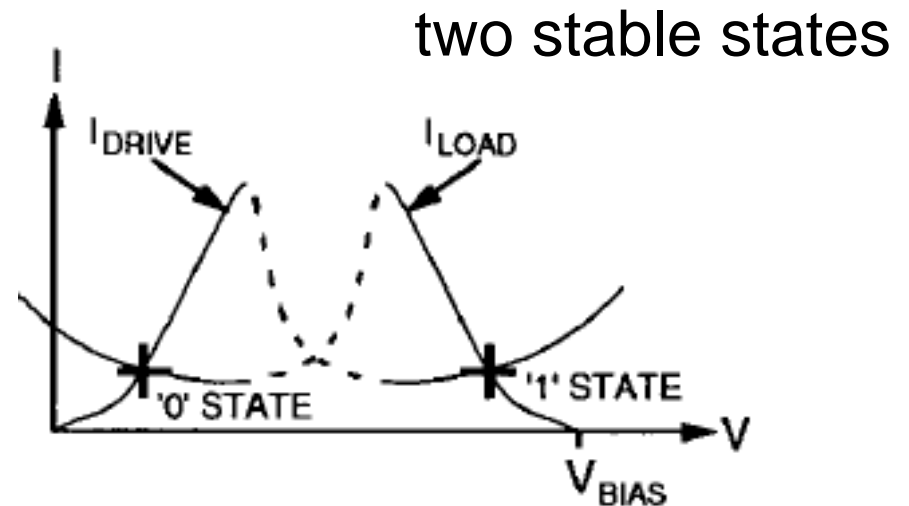
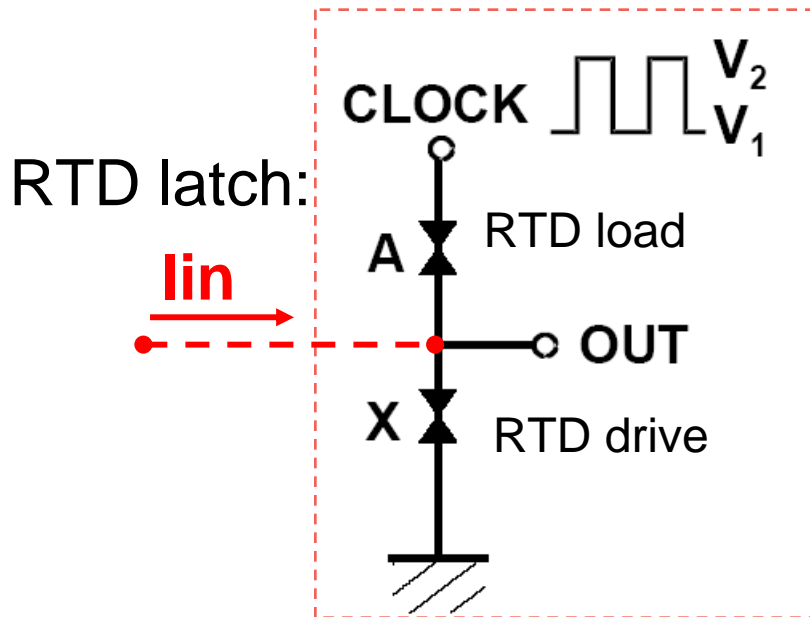


Inverter



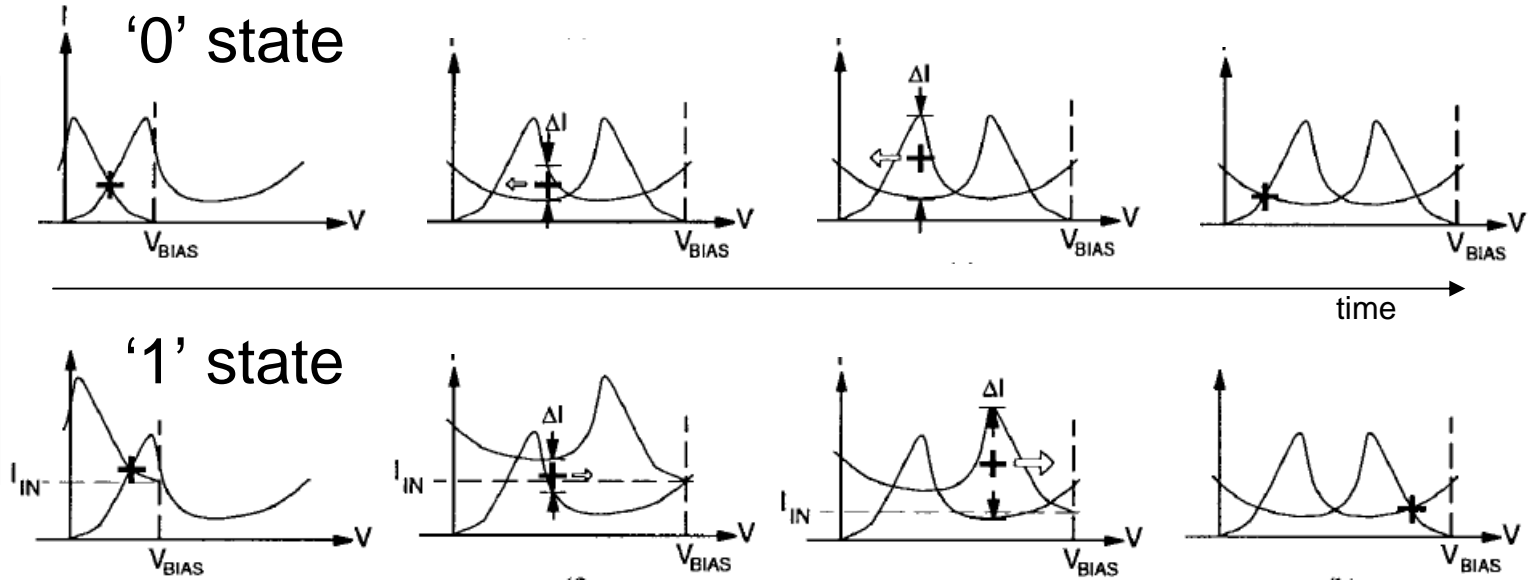
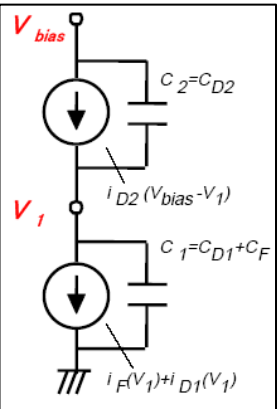
- Concept: A digital inverter cell with a low on-state current for low static power dissipation
- Evaluation: The low on-state current also reduces the switching speed because the current stays low until the RTD again reaches resonance

Monostable-bistable transition



- Voltage biasing two RTD's in series results in a bistable circuit.
- The state of a bistable pair is given by the voltage of the DATA NODE (OUT).
- the stable equilibrium states are labeled as "0" STATE and "1" STATE.

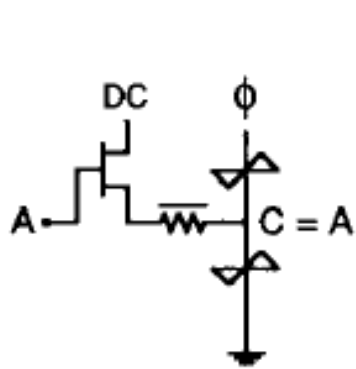
Non-equilibrium RTD-latch switching



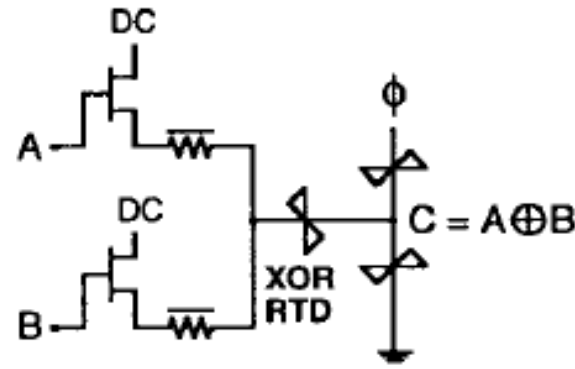
- To establish a new state in a latch, it must first be brought to a monostable bias and returned quickly to the bistable level.
- To set a latch to '1', an input current, I_{in} , must be supplied to the data node during the restoration of the bias voltage to the bistable level; otherwise: '0' the latch will be reset to the low-voltage state.
- When the total drive current is less than the drive-RTD conduction current, the capacitive current is negative and the voltage is driven lower.
- Likewise, when the total drive current is above the drive RTD conduction current, the voltage is driven higher.



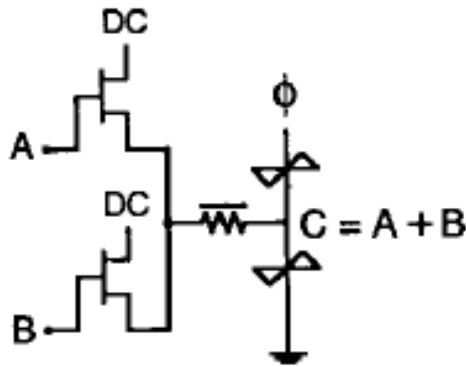
RTD logic gates



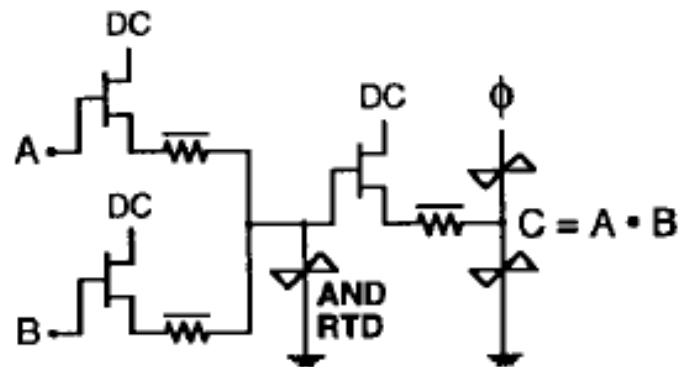
delay



XOR (NOT: one input kept 1)



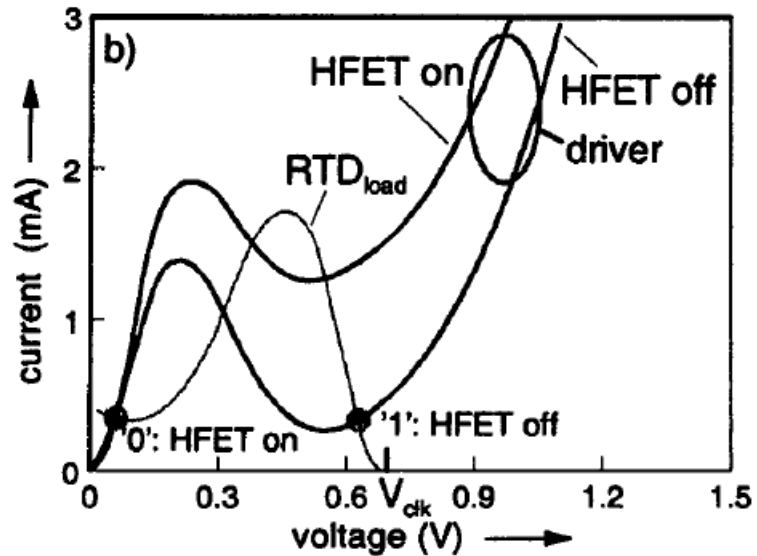
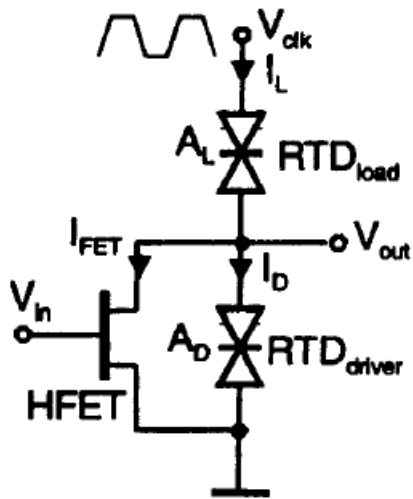
OR



AND



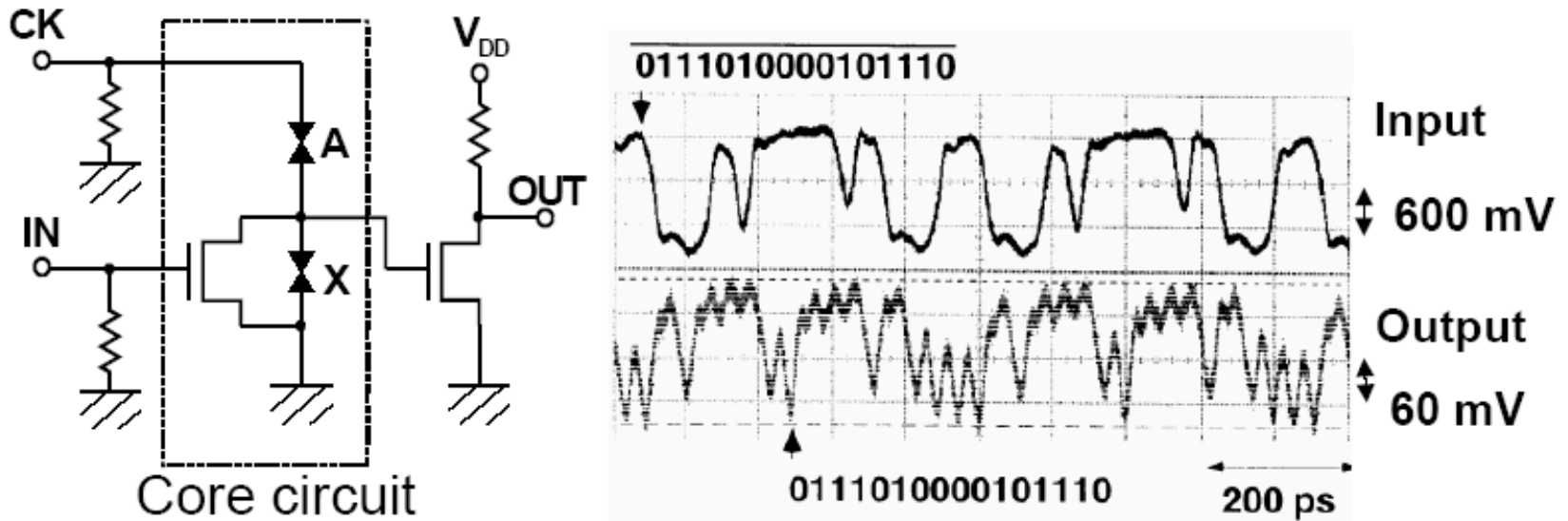
Monostable Bistable Logic Element (MOBILE)



- To establish a new state in a latch, it must first be brought to a monostable bias and returned quickly to the bistable level.
- To set a latch to '1', the HFET is OFF: if $A_L > A_D$, a net current charge the RTD driver capacitance, resulting in a switch toward the high voltage
- otherwise: the HFET is ON the net current in the DATA NODE is such that the capacitive current is negative and the voltage is driven lower.

MOBILE Flip-Flop Circuit Operating at up to 35 Gb/s

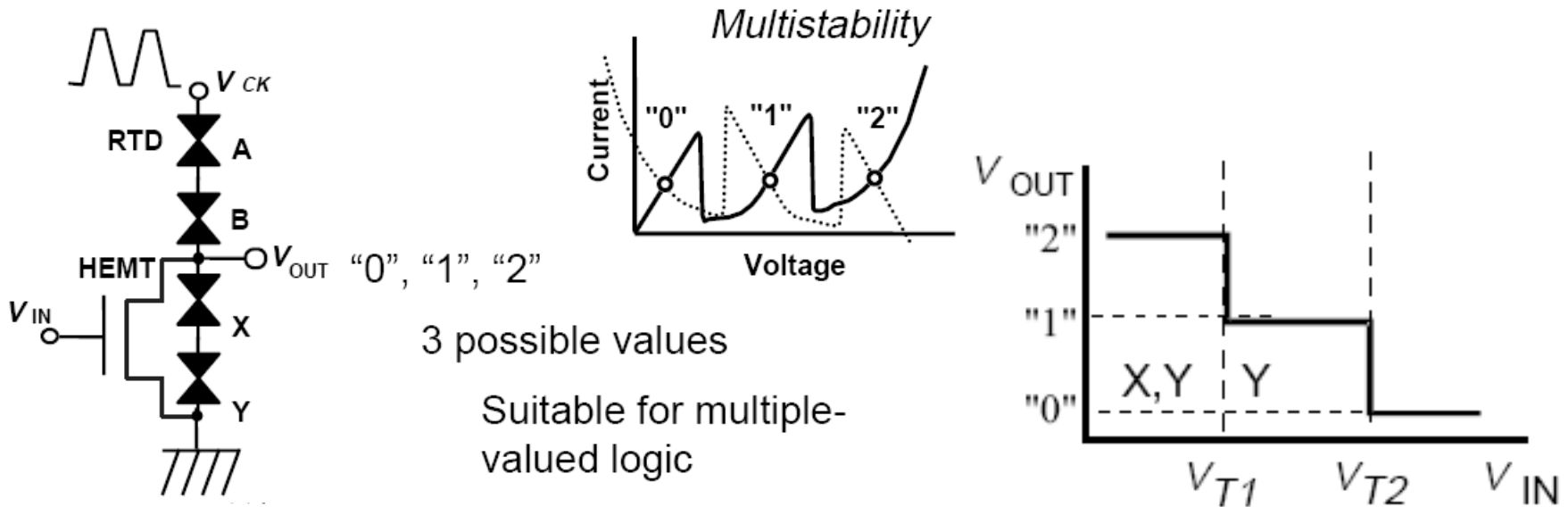
D-FF with RZ mode output



K. Maezawa et al., IEEE EDL,
vol. 19, no. 3, pp. 80 - 82, March 1998

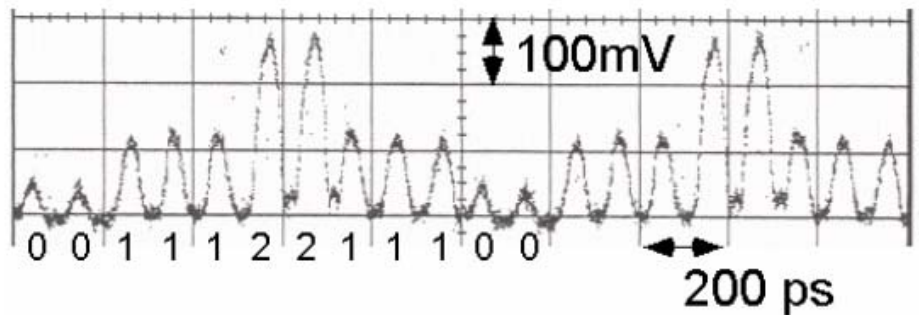
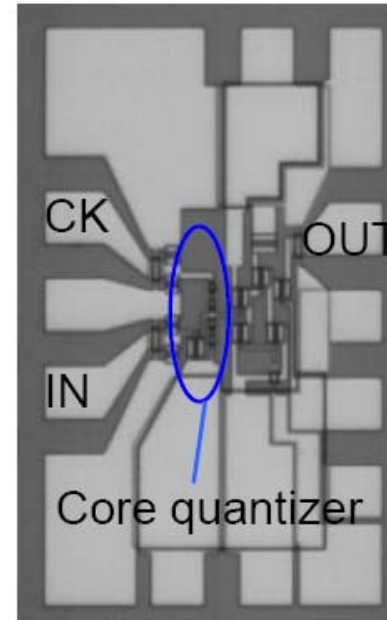
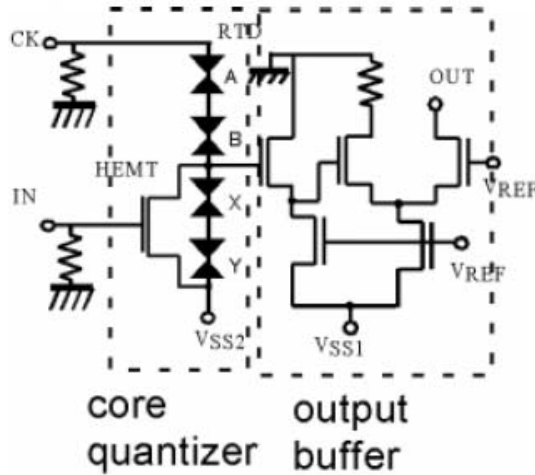
Multivalued Logic

- Operating Principle of Ternary Quantizer



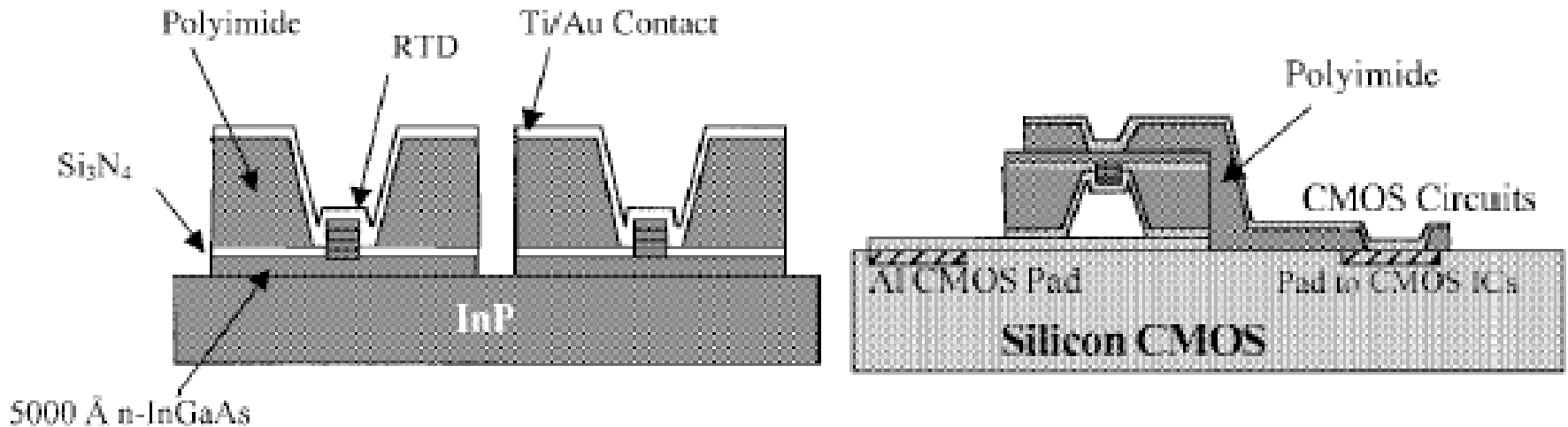
$$I_p(A) > I_p(B) > I_p(X) > I_p(Y)$$

Multivalued Logic

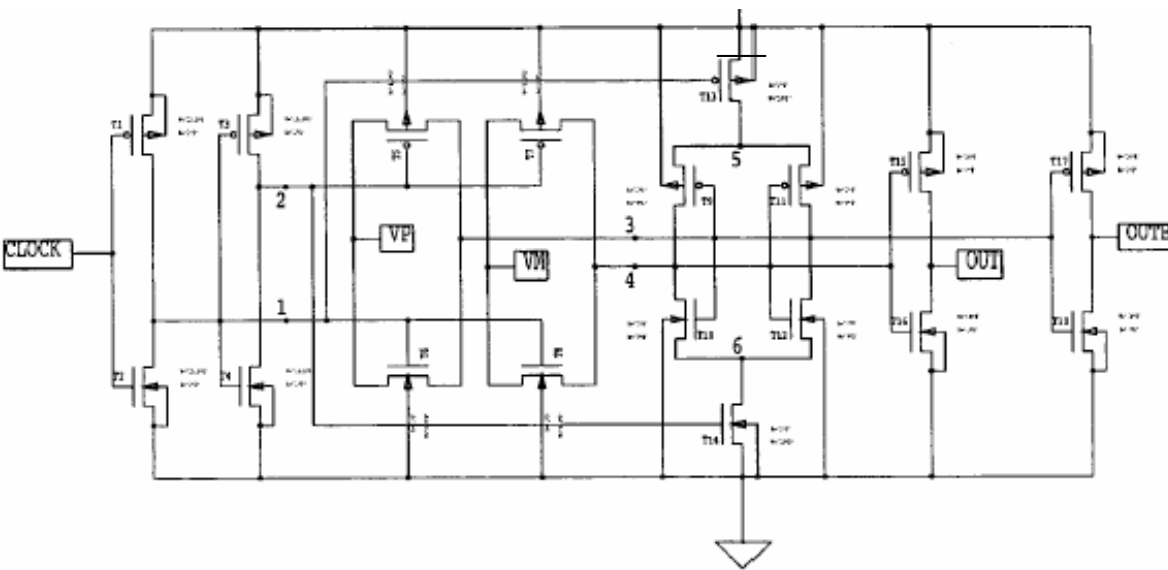


RTD-CMOS

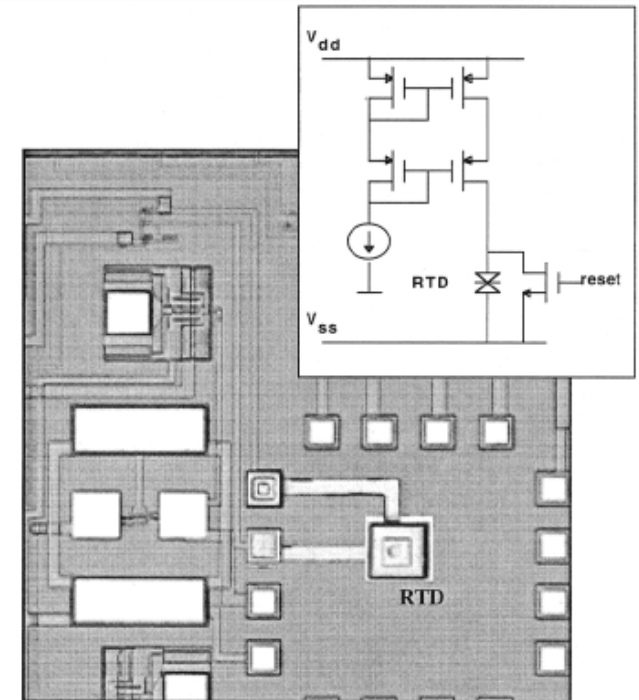
- Substantial improvement in speed, power dissipation, and circuit complexity over CMOS only circuits.
- A hybrid integration process for RTD to be transferred and bonded to CMOS



RTD-CMOS



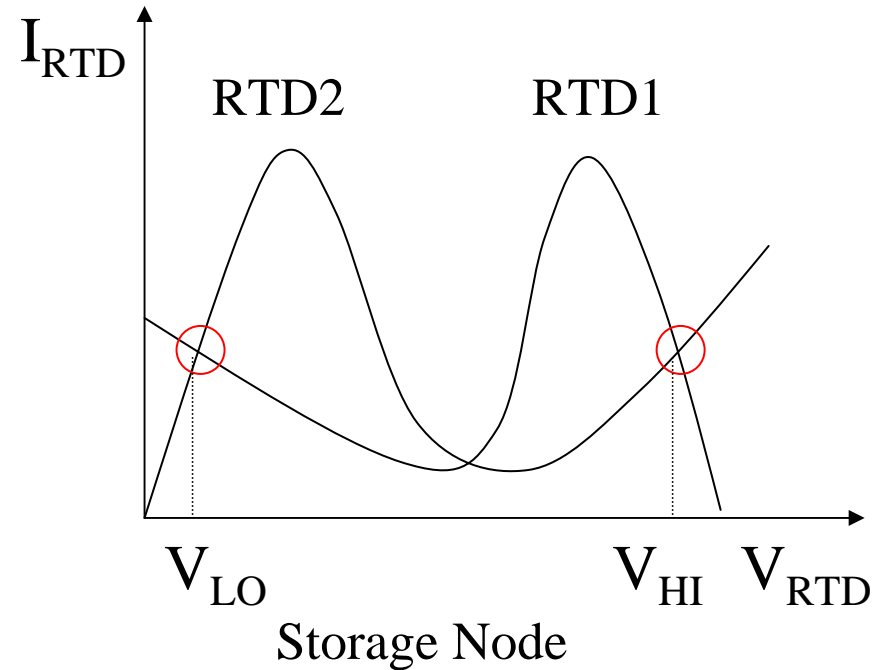
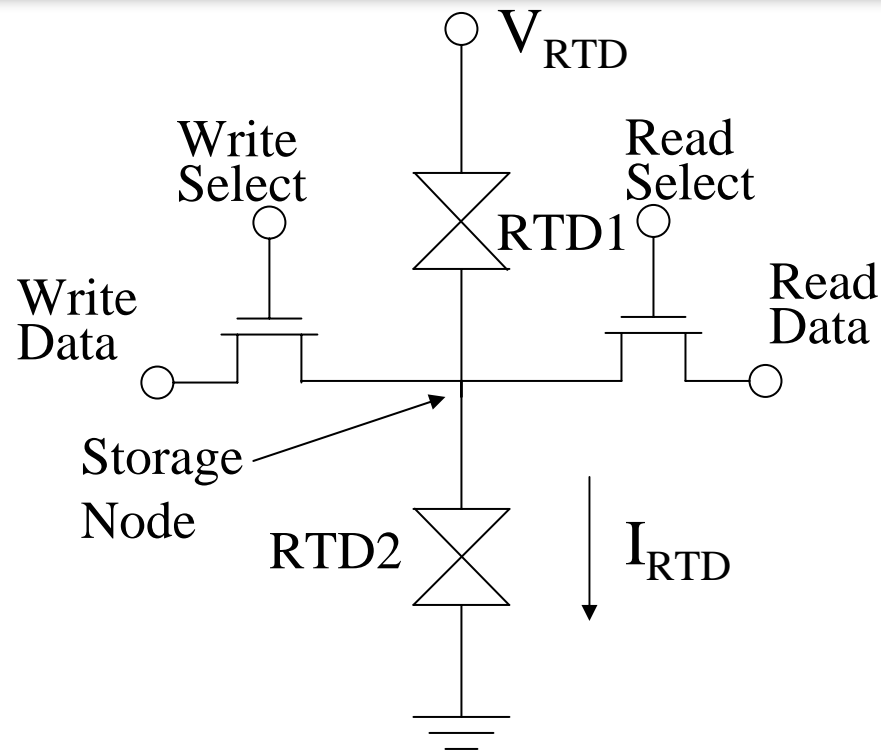
A 1-bit conventional CMOS comparator: 18 devices



A 1-bit RTD/CMOS comparator: 6 devices

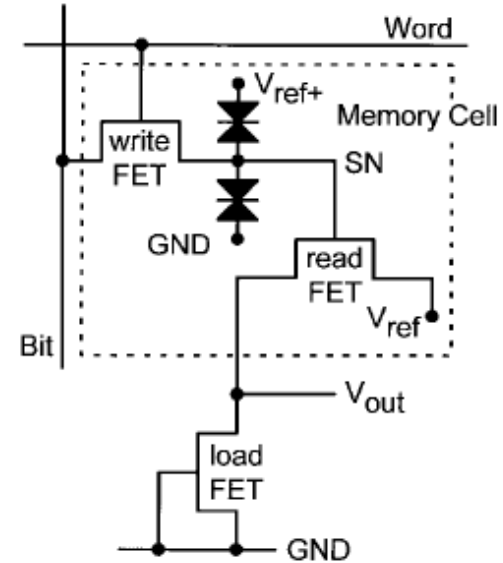
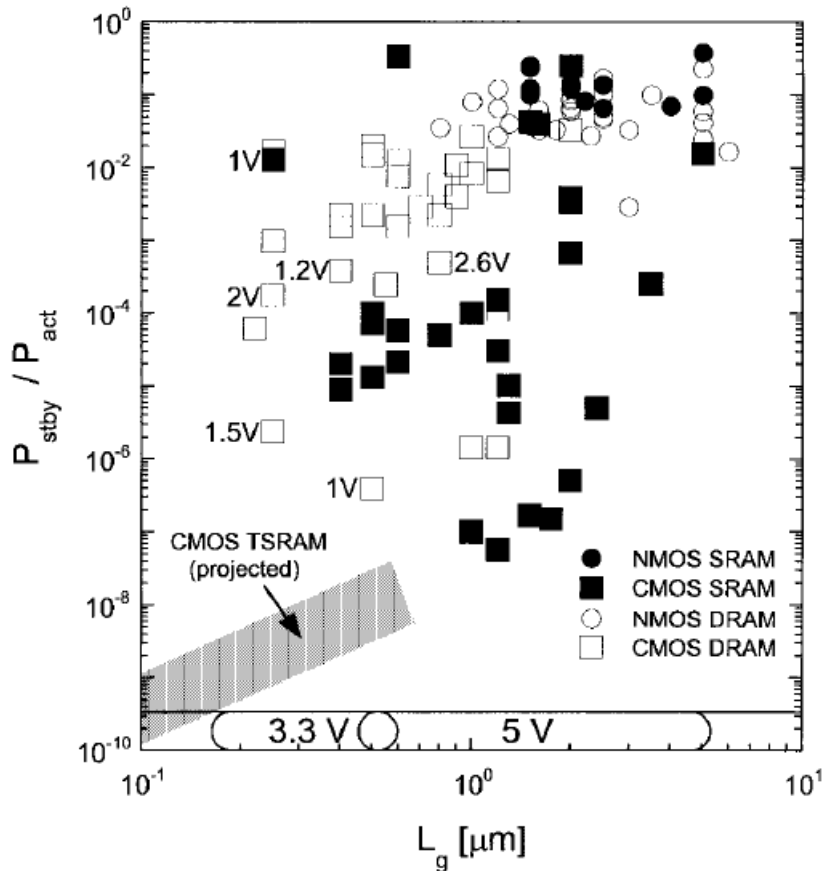
J. I. Bergman, et al., EDL, 1999

Memory cell



- **Concept: A static memory cell with a low device count and low static power dissipation**

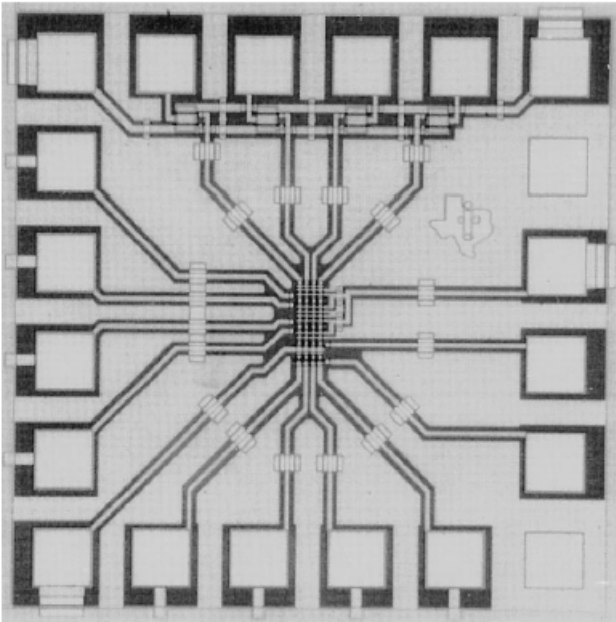
T-SRAM



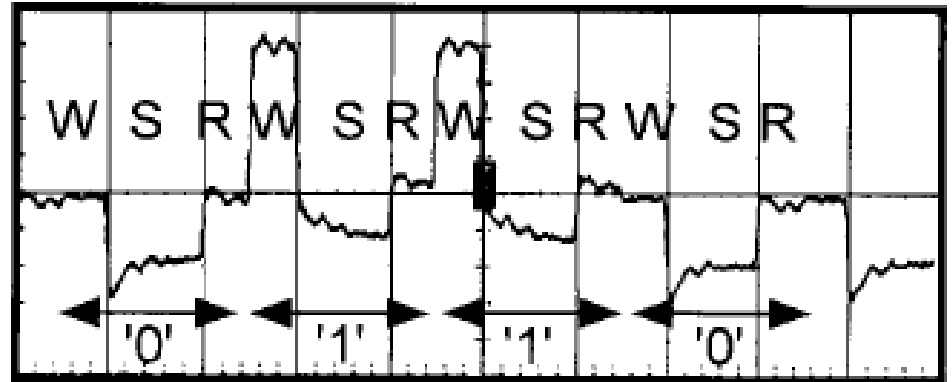
TSRAM cell test circuit.

V_{ref} is 1.0 V and RTD bias V_{ref+} is 0.45 V (2-state) or 1.0 V (3-state). The source follower at the storage node, SN, provides the read output V_{out} .

T-SRAM



Fabricated 4x4 1T-cell T-SRAM array.



Write–read cycles for high and low inputs for the 4x4-bit T-SRAM chip. Horizontal grid scale is 50 ns/div, vertical grid scale is 100 mV/div. The letters “W,” “S,” and “R” stand for write, store, and read, respectively.

Promising Future

